www.ietdl.org

Published in IET Power Electronics
Received on 8th July 2009
Revised on 13th September 2010
doi: 10.1049/iet-pel.2010.0210

ISSN 1755-4535

Design, modelling, control and simulation of a three-phase DC–DC converter for high currents applications

H.Y. Kanaan[1] *K. Al-Haddad*[2] *S. Georges*[3] *I. Mougharbel*[4]

[1]*Faculty of Engineering – ESIB, Saint-Joseph University, Campus des Sciences et Technologies, Mar Roukos, Mkallès B.P. 11-0514, Riad el Solh Beirut 1107 2050, Lebanon*
[2]*Canada Research Chair in Energy Conversion and Power Electronics, École de Technologie Supérieure (ETS), 1100 Rue Notre-Dame West, Montreal, Quebec, Canada H3C 1K3*
[3]*Notre-Dame University (NDU), P.O. Box 72, Zouk Mosbeh, Lebanon*
[4]*Faculty of Engineering, Lebanese University, Rafic Hariri Campus, Hadath, Lebanon*
E-mail: hadi.kanaan@usj.edu.lb

Abstract: In this study, a two-stage DC–DC converter for high current applications is studied. The converter consists of two three-phase full-bridge inverters connected through three AC coupled inductors. A switching-functions-based model of the converter is first established, and then a control scheme is designed for both inverters in order to ensure a high power factor at the AC stage, and a regulated voltage at the DC load. The performance of the proposed control system is verified through numerical simulations. First, an ideal DC source is considered in order to test the performance of the control system, then a proton exchange membrane fuel cell is applied as the DC source in order to highlight the usefulness of this converter in such applications.

1 Introduction

During the last two decades, several DC–DC topologies that cover a wide power range have been proposed. Most of them, based on the use of MOSFETs, were dedicated to low-power applications, and are generally provided with a high-frequency transformer that ensures galvanic isolation at the mid-stage [1]. In addition, the input stage of such converters is limited to a two-leg inverter, whereas the output stage consists only of rectifying diodes, yielding thus a unidirectional power flow.

In high-current applications, the use of two-leg topologies becomes insufficient, and the extension to the above-mentioned converters to the three-phase case becomes mandatory because of the limited ratings of the available semiconductors [2–5]. Furthermore, in order to decrease the current ratings in such converters without affecting the power level, a high-power factor is required at the AC mid-stage. This feature makes necessary the replacement of the conventional diode bridge output stage by a fully controlled six-switch rectifier. This topological modification will have other advantages: (i) the power flow becomes now bi-directional, (ii) the regulation of the DC voltage at the rectifier output becomes possible, (iii) the power losses in the cupper and the magnetic core are reduced, which is due essentially to the reduction of the root mean square (RMS)-currents and the elimination of low-frequency current harmonics, (iv) the power efficiency is consequently increased, (v) the size, weight and cost of the magnetic core are reduced and (vi) the electro-magnetic interference (EMI) disturbances become negligible.

The DC–DC topology considered in this paper is described in Fig. 1. It is generally used to connect two DC devices (which can be either sources or loads) that operate at different voltage levels. The converter consists of two six-switch inverters connected through three AC inductors. The resistors R represent the power losses in these inductors. The power flow in this structure is bi-directional; however, in the following study, the left-end is conventionally chosen as a source, whereas the right-end is considered as a load. Note that this convention will not affect the generality of the proposed study.

The inductors are designed on a same magnetic core, as depicted in Fig. 2. The bulkiness of the magnetic core could be easily and significantly reduced by increasing the fundamental frequency at the AC stage. Furthermore, because of the absence of a neutral connection at the AC level, the sum of the AC currents is always zero, and a fourth path for the zero-sequence flux in the magnetic core is not required.

Both six-switch bridges are controlled using the fixed-frequency carrier-based pulse-width-modulation technique [6]. The design of the regulators is elaborated according to the state model of two-stage converter. This model is established by using the switching-functions approach [7, 8]. The obtained model is then used to implement numerically the DC–DC converter transmission system in Matlab/Simulink.

Finally, the proposed control system is tested through simulations with a resistive load and for both cases of an ideal DC source and a proton exchange membrane fuel cell

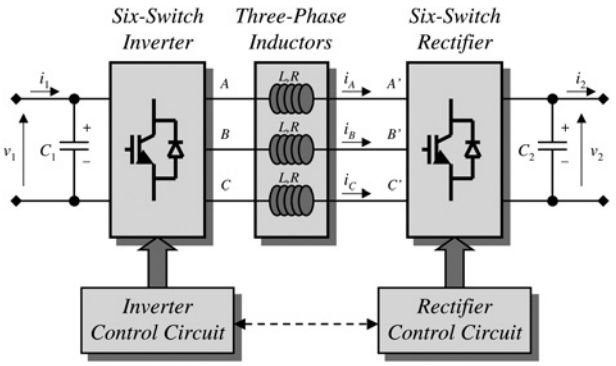


Fig. 1 *High-current two-stage DC–DC converter*

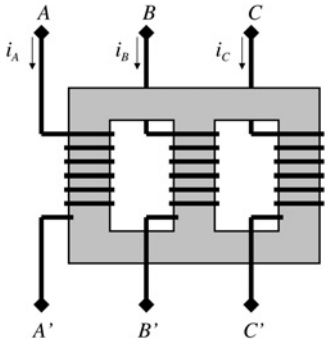


Fig. 2 *Three-phase inductors using a common magnetic core*

(PEMFC) source. For this latter case, a mathematical model of the PEMFC has been established and applied. The results have shown good performance of the converter regarding the DC-bus voltage stabilisation and the high-power quality on the AC-stage.

2 State-space modelling of the converter

2.1 Basic switching-functions-based model

All components in the basic study proposed in the paper are considered ideal, particularly the three-phase inductor where the unbalance of the magnetic circuit has been neglected for the sake of simplicity. In this case, the value of the inductor in phase A, that is L_A, is equal to $(L_{AA}-M)$ where L_{AA} denotes the auto-induction coefficient in phase A and M the mutual inductance that represents the effects of phases B and C on A. The inductor values in phases B and C are, in this case, both equal to L_A, which will be noted L in the following. Note that, by taking into account the asymmetry in the magnetic core, the model of the converter will be highly complicated making consequently the design of a suitable control system too difficult. The operation of the converter in the non-ideal case could be studied as a next step in a subsequent paper.

Considering the assumption made above, and by referring to Fig. 1, we may write the following equation for phase A

$$L\frac{\mathrm{d}i_A}{\mathrm{d}t} + Ri_A = v_A - v_{A'} \triangleq v_{AA'} \tag{1}$$

where i_A is the current in phase A, and $v_{AA'}$ is the voltage across the corresponding inductor, which may be composed as follows

$$v_{AA'} = v_{AO} + v_{OO'} - v_{A'O'} \tag{2}$$

O and O' are, respectively, the fictive mid-point at the DC input and output. Furthermore, referring to Fig. 3 that represents the internal structure of the input stage inverter, we have

$$v_{AO} = (s_A - \bar{s}_A)\cdot\frac{v_1}{2} \tag{3}$$

where v_1 denotes the input DC voltage and s_A the switching function of the upper switch Q_A, defined as

$$s_A = \begin{cases} 0, & \text{if } Q_A \text{ is turned off} \\ 1, & \text{if } Q_A \text{ is turned on} \end{cases} \tag{4}$$

and $\bar{s}_A$ is its logical complement. Similarly, knowing that the output stage converter has exactly the same structure as the input one, we also have

$$v_{A'O'} = (s'_A - \bar{s}'_A)\cdot\frac{v_2}{2} \tag{5}$$

where v_2 denotes the output DC voltage and s'_A the switching function of the rectifier upper switch connected to A'.

In the same manner, we can write for the other two phases the following equations

$$L\frac{\mathrm{d}i_B}{\mathrm{d}t} + Ri_B = v_{BB'} = v_{BO} + v_{OO'} - v_{B'O'} \tag{6}$$

and

$$L\frac{\mathrm{d}i_C}{\mathrm{d}t} + Ri_C = v_{CC'} = v_{CO} + v_{OO'} - v_{C'O'} \tag{7}$$

where

$$v_{BO} = (s_B - \bar{s}_B)\cdot\frac{v_1}{2} \tag{8}$$

$$v_{CO} = (s_C - \bar{s}_C)\cdot\frac{v_1}{2} \tag{9}$$

$$v_{B'O'} = (s'_B - \bar{s}'_B)\cdot\frac{v_2}{2} \tag{10}$$

$$v_{C'O'} = (s'_C - \bar{s}'_C)\cdot\frac{v_2}{2} \tag{11}$$

s_B and s_C being the switching functions of the inverter upper

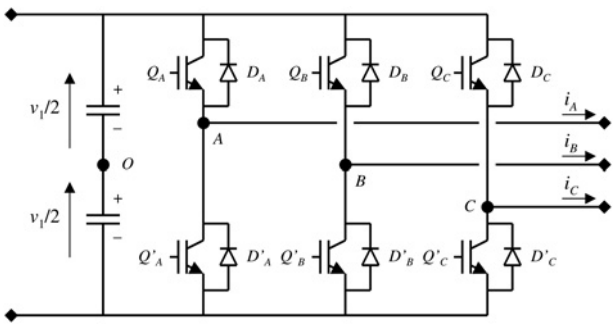


Fig. 3 *Input stage inverter*

switches connected to nodes B and C, respectively, s'_B and s'_C the switching functions of the rectifier upper switches connected to nodes B' and C', respectively.

Furthermore, the neutral at the AC mid-stage being disconnected, it follows that the zero-sequence in the AC currents (and consequently in the voltages across the inductors) is always equal to zero, that is

$$i_A(t) + i_B(t) + i_C(t) \equiv 0, \quad \forall t \tag{12}$$

and

$$v_{AA'}(t) + v_{BB'}(t) + v_{CC'}(t) \equiv 0, \quad \forall t \tag{13}$$

Combining (13) with (2), (6) and (7) yields

$$v_{OO'} = -\frac{1}{3}[(v_{AO} + v_{BO} + v_{CO}) - (v_{A'O'} + v_{B'O'} + v_{C'O'})] \tag{14}$$

In addition, regarding the DC output stage of the converter, we have the following

$$C_2 \frac{\mathrm{d}v_2}{\mathrm{d}t} = s'_A i_A + s'_B i_B + s'_C i_C - i_2 \tag{15}$$

i_2 denoting the DC output current.

The state equations of the converter given in (1), (6), (7) and (15) can be grouped and rewritten in a matrix form as

$$L\frac{\mathrm{d}\boldsymbol{i}_{\boldsymbol{ABC}}}{\mathrm{d}t} + R\boldsymbol{i}_{\boldsymbol{ABC}} = \boldsymbol{\Gamma}(\boldsymbol{v}_{\boldsymbol{ABCO}} - \boldsymbol{v}'_{\boldsymbol{ABCO}}) \tag{16}$$

and

$$C_2 \frac{\mathrm{d}v_2}{\mathrm{d}t} = \boldsymbol{s}'^{\mathrm{T}}_{\boldsymbol{ABC}} \cdot \boldsymbol{i}_{\boldsymbol{ABC}} - i_2 \tag{17}$$

where

$$\boldsymbol{\Gamma} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \tag{18}$$

$$\boldsymbol{v}_{\boldsymbol{ABCO}} = (\boldsymbol{s}_{\boldsymbol{ABC}} - \bar{\boldsymbol{s}}_{\boldsymbol{ABC}}) \cdot \frac{v_1}{2} \tag{19}$$

$$\boldsymbol{v}'_{\boldsymbol{ABCO}} = (\boldsymbol{s}'_{\boldsymbol{ABC}} - \bar{\boldsymbol{s}}'_{\boldsymbol{ABC}}) \cdot \frac{v_2}{2} \tag{20}$$

$\boldsymbol{i}_{\boldsymbol{ABC}} = [i_A, i_B, i_C]^{\mathrm{T}}$ is the current vector, $\boldsymbol{v}_{\boldsymbol{ABCO}} = [v_{AO}, v_{BO}, v_{CO}]^{\mathrm{T}}$ the voltage vector at the inverter AC side, $\boldsymbol{v}'_{\boldsymbol{ABCO}} = [v_{A'O'}, v_{B'O'}, v_{C'O'}]^{\mathrm{T}}$ the voltage vector at the rectifier AC side, $\boldsymbol{s}_{\boldsymbol{ABC}} = [s_A, s_B, s_C]^{\mathrm{T}}$ the switching functions vector of the inverter upper switches and $\boldsymbol{s}'_{\boldsymbol{ABC}} = [s'_A, s'_B, s'_C]^{\mathrm{T}}$ the switching functions vector of the rectifier upper switches.

The system characterised by (16) and (17) represents the basic state model of the converter in the stationary frame. The system order can be reduced by applying Park's transformation, as discussed in the next sub-section.

2.2 Frame transformation

The model defined by (16) and (17) can be expressed in a new rotating frame using Park's transformation. The Park's matrix is defined as [6]

$$\boldsymbol{K} = \frac{2}{3}\begin{bmatrix} \sin(\omega t) & \sin(\omega t - 2\pi/3) & \sin(\omega t - 4\pi/3) \\ \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t - 4\pi/3) \\ 3/2 & 3/2 & 3/2 \end{bmatrix} \tag{21}$$

where ω is the angular frequency of the AC variables. By defining the new vectors $\boldsymbol{i}^{\boldsymbol{r}}_{\boldsymbol{ABC}}$, $\boldsymbol{v}^{\boldsymbol{r}}_{\boldsymbol{ABCO}}$, $\boldsymbol{v}'^{\boldsymbol{r}}_{\boldsymbol{ABCO}}$, $\boldsymbol{s}^{\boldsymbol{r}}_{\boldsymbol{ABC}}$ and $\boldsymbol{s}'^{\boldsymbol{r}}_{\boldsymbol{ABC}}$ as follows

$$\boldsymbol{i}^{\boldsymbol{r}}_{\boldsymbol{ABC}} \triangleq \begin{bmatrix} i_d & i_q & i_0 \end{bmatrix}^{\mathrm{T}} = \boldsymbol{K}\boldsymbol{i}_{\boldsymbol{ABC}} \tag{22a}$$

$$\boldsymbol{v}^{\boldsymbol{r}}_{\boldsymbol{ABCO}} \triangleq \begin{bmatrix} v_d & v_q & v_0 \end{bmatrix}^{\mathrm{T}} = \boldsymbol{K}\boldsymbol{v}_{\boldsymbol{ABCO}} \tag{22b}$$

$$\boldsymbol{v}'^{\boldsymbol{r}}_{\boldsymbol{ABCO}} \triangleq \begin{bmatrix} v'_d & v'_q & v'_0 \end{bmatrix}^{\mathrm{T}} = \boldsymbol{K}\boldsymbol{v}'_{\boldsymbol{ABCO}} \tag{22c}$$

$$\boldsymbol{s}^{\boldsymbol{r}}_{\boldsymbol{ABC}} \triangleq \begin{bmatrix} s_d & s_q & s_0 \end{bmatrix}^{\mathrm{T}} = \boldsymbol{K}\boldsymbol{s}_{\boldsymbol{ABC}} \tag{22d}$$

$$\boldsymbol{s}'^{\boldsymbol{r}}_{\boldsymbol{ABC}} \triangleq \begin{bmatrix} s'_d & s'_q & s'_0 \end{bmatrix}^{\mathrm{T}} = \boldsymbol{K}\boldsymbol{s}'_{\boldsymbol{ABC}} \tag{22e}$$

equations (16), (17), (19) and (20) can be arranged as

$$L\left(\boldsymbol{K}\frac{\mathrm{d}\boldsymbol{K}^{-1}}{\mathrm{d}t}\right)\boldsymbol{i}^{\boldsymbol{r}}_{\boldsymbol{ABC}} + L\frac{\mathrm{d}\boldsymbol{i}^{\boldsymbol{r}}_{\boldsymbol{ABC}}}{\mathrm{d}t} + R\boldsymbol{i}^{\boldsymbol{r}}_{\boldsymbol{ABC}} = (\boldsymbol{K}\cdot\boldsymbol{\Gamma}\cdot\boldsymbol{K}^{-1})\cdot(\boldsymbol{v}^{\boldsymbol{r}}_{\boldsymbol{ABCO}} - \boldsymbol{v}'^{\boldsymbol{r}}_{\boldsymbol{ABCO}}) \tag{23}$$

$$C_2\frac{\mathrm{d}v_2}{\mathrm{d}t} = (\boldsymbol{s}'^{\boldsymbol{r}}_{\boldsymbol{ABC}})^{\boldsymbol{T}}\cdot(\boldsymbol{K}\boldsymbol{K}^{\boldsymbol{T}})^{-1}\cdot\boldsymbol{i}^{\boldsymbol{r}}_{\boldsymbol{ABC}} - i_2 \tag{24}$$

$$\boldsymbol{v}^{\boldsymbol{r}}_{\boldsymbol{ABCO}} = (\boldsymbol{s}^{\boldsymbol{r}}_{\boldsymbol{ABC}} - \boldsymbol{K}\cdot\bar{\boldsymbol{s}}_{\boldsymbol{ABC}})\cdot\frac{v_1}{2} \tag{25}$$

$$\boldsymbol{v}'^{\boldsymbol{r}}_{\boldsymbol{ABCO}} = (\boldsymbol{s}'^{\boldsymbol{r}}_{\boldsymbol{ABC}} - \boldsymbol{K}\cdot\bar{\boldsymbol{s}}'_{\boldsymbol{ABC}})\cdot\frac{v_2}{2} \tag{26}$$

Using the following properties

$$\boldsymbol{K}\frac{\mathrm{d}\boldsymbol{K}^{-1}}{\mathrm{d}t} = \omega\cdot\begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{27}$$

$$\boldsymbol{K}\cdot\boldsymbol{\Gamma}\cdot\boldsymbol{K}^{-1} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{28}$$

$$(\boldsymbol{K}\boldsymbol{K}^{\boldsymbol{T}})^{-1} = \begin{bmatrix} 3/2 & 0 & 0 \\ 0 & 3/2 & 0 \\ 0 & 0 & 1/3 \end{bmatrix} \tag{29}$$

$$\boldsymbol{K}\cdot\bar{\boldsymbol{s}}_{\boldsymbol{ABC}} = \boldsymbol{K}\cdot\begin{bmatrix} 1 & 1 & 1 \end{bmatrix}^{\mathrm{T}} - \boldsymbol{s}^{\boldsymbol{r}}_{\boldsymbol{ABC}} = \begin{bmatrix} 0 & 0 & 3 \end{bmatrix}^{\mathrm{T}} - \boldsymbol{s}^{\boldsymbol{r}}_{\boldsymbol{ABC}} \tag{30}$$

$$\boldsymbol{K}\cdot\bar{\boldsymbol{s}}'_{\boldsymbol{ABC}} = \boldsymbol{K}\cdot\begin{bmatrix} 1 & 1 & 1 \end{bmatrix}^{\mathrm{T}} - \boldsymbol{s}'^{\boldsymbol{r}}_{\boldsymbol{ABC}} = \begin{bmatrix} 0 & 0 & 3 \end{bmatrix}^{\mathrm{T}} - \boldsymbol{s}'^{\boldsymbol{r}}_{\boldsymbol{ABC}} \tag{31}$$

doi: 10.1049/iet-pel.2010.0210

into (23) to (26) yields

$$L\frac{\mathrm{d}i_d}{\mathrm{d}t} = -Ri_d + L\omega i_q + v_d - v'_d \tag{32}$$

$$L\frac{\mathrm{d}i_q}{\mathrm{d}t} = -Ri_q - L\omega i_d + v_q - v'_q \tag{33}$$

$$C_2\frac{\mathrm{d}v_2}{\mathrm{d}t} = \frac{3}{2}(s'_d i_d + s'_q i_q) - i_2 \tag{34}$$

with

$$v_d = s_d v_1 \tag{35}$$

$$v_q = s_q v_1 \tag{36}$$

$$v'_d = s'_d v_2 \tag{37}$$

$$v'_q = s'_q v_2 \tag{38}$$

As for the voltage zero sequences v_0 and v'_0, they are given as

$$v_0 = s_0 v_1 - \frac{3}{2}v_1 \tag{39}$$

$$v'_0 = s'_0 v_2 - \frac{3}{2}v_2 \tag{40}$$

2.3 State-space-averaged model

By adopting a same switching frequency for both six-switch bridges, and by introducing the duty cycle vectors $\boldsymbol{d_{ABC}} = [d_A,\ d_B,\ d_C]^{\mathrm{T}}$ and $\boldsymbol{d'_{ABC}} = [d'_A,\ d'_B,\ d'_C]^{\mathrm{T}}$ for the upper switches in the input stage inverter and output stage rectifier, respectively, we can easily deduce the state-space average model of the converter by averaging all variables in (32)–(38) over a switching period T_S. It yields

$$L\frac{\mathrm{d}i_d}{\mathrm{d}t} = -Ri_d + L\omega i_q + d_d v_1 - d'_d v_2 \tag{41}$$

$$L\frac{\mathrm{d}i_q}{\mathrm{d}t} = -Ri_q - L\omega i_d + d_q v_1 - d'_q v_2 \tag{42}$$

$$C_2\frac{\mathrm{d}v_2}{\mathrm{d}t} = \frac{3}{2}(d'_d i_d + d'_q i_q) - i_2 \tag{43}$$

where

$$\boldsymbol{d^r_{ABC}} \triangleq \begin{bmatrix} d_d & d_q & d_0 \end{bmatrix}^{\mathrm{T}} = \boldsymbol{K d_{ABC}} \tag{44}$$

$$\boldsymbol{d'^r_{ABC}} \triangleq \begin{bmatrix} d'_d & d'_q & d'_0 \end{bmatrix}^{\mathrm{T}} = \boldsymbol{K d'_{ABC}} \tag{45}$$

The zero-sequence components d_0 and d'_0 of both sets of duty cycles can be derived, respectively, from (39) and (40) as follows

$$d_0 = \frac{3}{2} + \frac{v_0}{v_1} = \frac{3}{2} + \frac{v_{AO} + v_{BO} + v_{CO}}{v_1} \tag{46}$$

$$d'_0 = \frac{3}{2} + \frac{v'_0}{v_2} = \frac{3}{2} + \frac{v_{A'O'} + v_{B'O'} + v_{C'O'}}{v_2} \tag{47}$$

Equations (41) to (43) show that the converter in Fig. 1 can be represented in the low-frequency domain by a third-order non-linear dynamic system, having i_d, i_q and v_2 as the state or output variables, d_d, d_q, d'_d and d'_q as the control inputs.

3 Control strategy

3.1 Inverter control design

The system outputs could be all adjusted by controlling properly only the output stage rectifier. In this case, the inverter control becomes quite simple, and would consist only of an open loop gate signals generation using the conventional sine-triangle pulse-width-modulation technique. Hence, by denoting u_A, u_B and u_C the inverter reference signals defined as

$$\begin{aligned} u_A(t) &= \hat{u}\cdot\sin(\omega t) \\ u_B(t) &= \hat{u}\cdot\sin(\omega t - 2\pi/3) \\ u_C(t) &= \hat{u}\cdot\sin(\omega t - 4\pi/3) \end{aligned} \tag{48}$$

which would be compared to a common high-frequency triangular carrier with a peak value $\hat{v}_{\mathrm{tri}}$, the expressions of the duty cycles that correspond to the inverter upper switches become in the stationary frame

$$\begin{aligned} d_A(t) &= \frac{1}{2} + \frac{r}{2}\sin(\omega t) \\ d_B(t) &= \frac{1}{2} + \frac{r}{2}\sin(\omega t - 2\pi/3) \\ d_C(t) &= \frac{1}{2} + \frac{r}{2}\sin(\omega t - 4\pi/3) \end{aligned} \tag{49}$$

and in the rotating frame

$$\begin{aligned} d_d &= \frac{r}{2} \\ d_q &= 0 \\ d_0 &= \frac{3}{2} \end{aligned} \tag{50}$$

where $r = \hat{u}/\hat{v}_{\mathrm{tri}}$ denotes the voltage regulation parameter.

Furthermore, in order to minimise the current constraints at rated power consumption, the parameter r is set to its maximum value $r_{\max} = 1$.

3.2 Rectifier control design

A multiple-loop linear control system is designed for the rectifier using the averaged model in the rotating frame given in Section 2.3. The control scheme is presented in Fig. 4. $\boldsymbol{K}$ represents the stationary/synchronous frame transformation. The current references i^*_d and i^*_q are generated as follows

$$\begin{aligned} i^*_d &= \frac{\hat{i}^*}{\sqrt{v^2_{d,0} + v^2_{q,0}}} v_{d,0} \\ i^*_q &= \frac{\hat{i}^*}{\sqrt{v^2_{d,0} + v^2_{q,0}}} v_{q,0} \end{aligned} \tag{51}$$

where $\hat{i}^*$ denotes the peak value of the reference currents, $v_{d,0}$ and $v_{q,0}$ are, respectively, the DC-components of v_d and v_q.

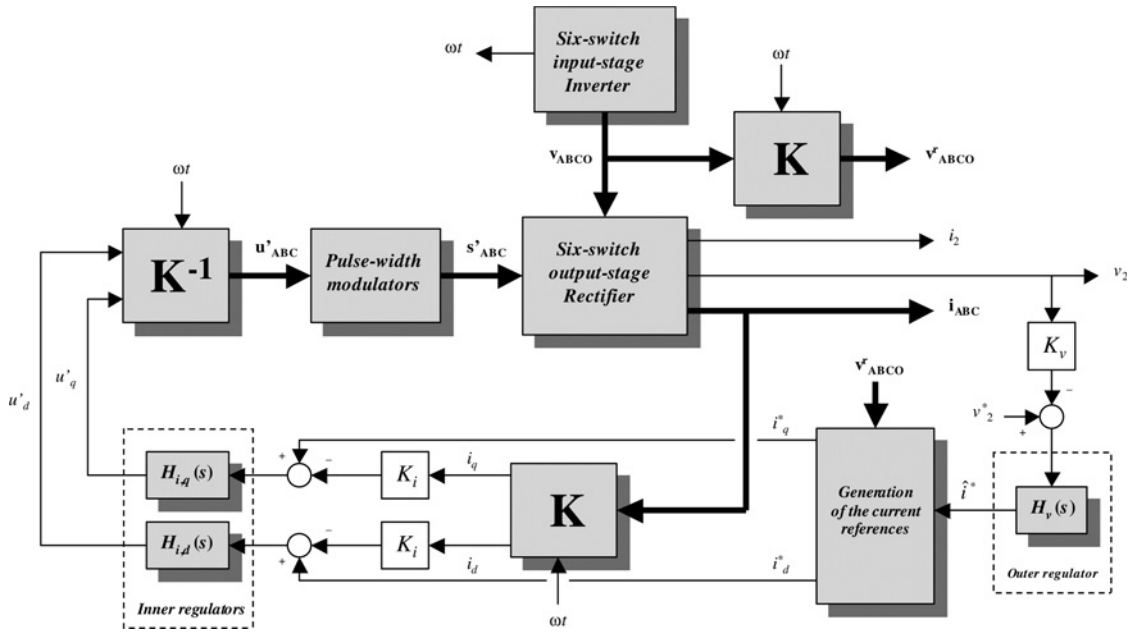


Fig. 4 *Rectifier control scheme*

Note that these components represent also the fundamental voltage at the inverter output.

In a control point of view, it should be mentioned that the system's outputs i_d, i_q and v_2 are not independent. They are related in particular through the energy conservation law. So, theoretically, only two of them can be controlled directly by the duty cycles d'_d and d'_q. This fact was considered in the design of the scheme. In fact, as illustrated in Fig. 4, only i_d and i_q are controlled directly by the control inputs (i.e. the duty cycles). The remaining output v_2 is regulated by an external feedback loop, through the adjustment of the AC currents peak value.

K_i and K_v are, respectively, the current and voltage loops feedback-scaling gains. The proportional-integral-type inner regulators $H_{i,d}(s)$, $H_{i,q}(s)$ and outer regulator $H_v(s)$ are designed independently by using the successive feedback looping approach described in [9]. That means that all the cross-coupling between the control inputs and the system outputs was not considered. In fact, as seen from (41) to (43), the converter model is a multi-input-multi-output one, which means that each output depends on all input variables at once. One simple and forward method for designing the inner control loops, as suggested in [9], is to consider only the transfer functions that relate i_d to d'_d in one hand, and i_q to d'_q in the other. The effects of d'_d and d'_q on i_q and i_d, respectively, are considered as disturbances in the control design process. The control outputs u'_A, u'_B and u'_C are then compared to the high-frequency triangular carrier in order to generate the rectifier gate signals.

On the other hand, the outer loop is designed to be slower enough than the inner ones in order to ensure high stability to the control system.

4 Output voltage setting

In order to preserve a maximum tracking ability for the AC currents and allow them to follow in the average their corresponding references, a suitable choice of the DC output voltage v_2 is required.

As described in Fig. 5, the time variation of the current i_A in phase A is mainly controlled by the state of switch $Q_{A'}$ (which

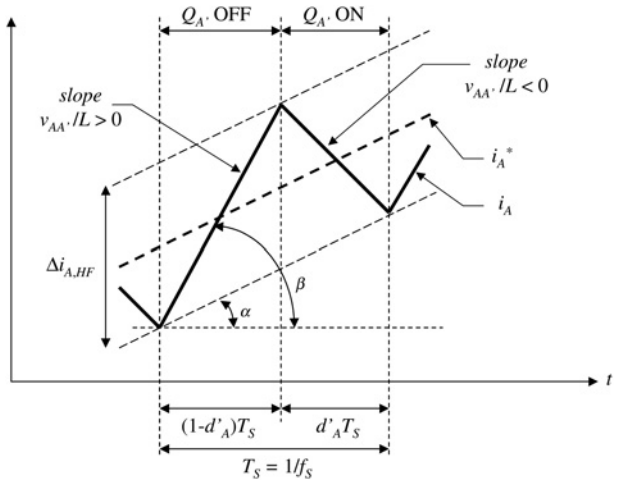


Fig. 5 *Waveform of current in phase A over a switching period*

is the upper switch in the rectifier, connected to A'). $\Delta i_{A,\mathrm{HF}}$ represents the ripple of current i_A at the switching frequency, and the angles α and β are defined as follows

$$\tan(\alpha) = \frac{\mathrm{d}i_A^*(t)}{\mathrm{d}t} \tag{52}$$

$$\tan(\beta) = \frac{v_{AA'}}{L} \tag{53}$$

It is clearly deduced from Fig. 5 that the current modulation ability is maintained as long as the following conditions are satisfied

$$v_{AA'} > 0 \quad \text{if } Q_{A'} \text{ is OFF} \tag{54}$$

and

$$v_{AA'} < 0 \quad \text{if } Q_{A'} \text{ is ON} \tag{55}$$

Note that in the construction of Fig. 5 and the derivation of expressions (53)–(55), it was assumed that the series

doi: 10.1049/iet-pel.2010.0210

resistance R of the inductors is negligible, which is the case in practice.

Referring to Table 1 that gives the expressions of $v_{AA'}$ for all possible switching configurations provided that $Q_{A'}$ is turned-off, condition (54) implies that maximum tracking ability is attained if

$$v_2(t) > 2v_1(t), \quad \forall t \tag{56}$$

The same result is obtained if we had considered the on-state of switch $Q_{A'}$ rather the off-state. In that case, s'_A is always equal to 1, and a term $(-2v_2/3)$ should be added in all expressions of the last column in Table 1. This result is also obtainable if the above analysis had been applied on current i_B or i_C instead of i_A. Note that, in Table 1, all configurations that correspond to a negative value of $v_{AA'}$ at $Q_{A'}$ OFF would cause a control detuning problem and the saturation of the control inputs.

The inductors value also affects the tracking ability of the phase currents. It should comply with the following constraint

$$\min(|\tan(\beta)|) > \max(|\tan(\alpha)|) \tag{57}$$

Using (52) and (53), and referring to Table 1, it yields

$$L < \frac{\min(v_2 - 2v_1, v_1)}{3 \cdot \max(|\mathrm{d}i_A^*(t)/\mathrm{d}t|)} \triangleq L_{\max} \tag{58}$$

If the current reference i_A^* is a sine-wave (which is the case in this application), expression (58) would become

$$L_{\max} = \frac{\min(v_2 - 2v_1, v_1)}{3\hat{i}^* \omega} \tag{59}$$

where $\hat{i}^*$ denotes the peak value of i_A^* and ω its angular frequency.

5 Simulation results

5.1 Case of an ideal DC source

The system in Fig. 1 and its control circuit are implemented in Matlab/Simulink. The numerical values of the system parameters are given in Appendix 1. A resistive load is connected at the rectifier DC output, and an ideal DC source is applied at the inverter input. The operating set point is chosen as follows:

DC source voltage $v_1 = 100$ V;
desired DC load voltage $v_2^* = 400$ V;
rated load power $P = 25$ kW.

The capacitor C_1 is omitted. The simulations carried out in this study are limited to the case where the power flow is unidirectional. Further analysis and simulations related to more general cases will be reported subsequent papers. The

Table 1 Expressions of the voltage across the inductor of phase A when $Q_{A'}$ is off

s_A	s_B	s_C	s'_A	s'_B	s'_C	v_{AO}	v_{BO}	v_{CO}	$v_{A'O'}$	$v_{B'O'}$	$v_{C'O'}$	$v_{OO'}$	$v_{AA'}$
1	1	1	0	0	0	$v_1/2$	$v_1/2$	$v_1/2$	$-v_2/2$	$-v_2/2$	$-v_2/2$	$-v_1/2-v_2/2$	0
1	1	0	0	0	0	$v_1/2$	$v_1/2$	$-v_1/2$	$-v_2/2$	$-v_2/2$	$-v_2/2$	$-v_1/6-v_2/2$	$v_1/3$
1	0	1	0	0	0	$v_1/2$	$-v_1/2$	$v_1/2$	$-v_2/2$	$-v_2/2$	$-v_2/2$	$-v_1/6-v_2/2$	$v_1/3$
1	0	0	0	0	0	$v_1/2$	$-v_1/2$	$-v_1/2$	$-v_2/2$	$-v_2/2$	$-v_2/2$	$v_1/6-v_2/2$	$2v_1/3$
0	1	1	0	0	0	$-v_1/2$	$v_1/2$	$v_1/2$	$-v_2/2$	$-v_2/2$	$-v_2/2$	$-v_1/6-v_2/2$	$-2v_1/3$
0	1	0	0	0	0	$-v_1/2$	$v_1/2$	$-v_1/2$	$-v_2/2$	$-v_2/2$	$-v_2/2$	$v_1/6-v_2/2$	$-v_1/3$
0	0	1	0	0	0	$-v_1/2$	$-v_1/2$	$v_1/2$	$-v_2/2$	$-v_2/2$	$-v_2/2$	$v_1/6-v_2/2$	$-v_1/3$
0	0	0	0	0	0	$-v_1/2$	$-v_1/2$	$-v_1/2$	$-v_2/2$	$-v_2/2$	$-v_2/2$	$v_1/2-v_2/2$	0
1	1	1	0	0	1	$v_1/2$	$v_1/2$	$v_1/2$	$-v_2/2$	$-v_2/2$	$v_2/2$	$-v_1/2-v_2/6$	$v_2/3$
1	1	0	0	0	1	$v_1/2$	$v_1/2$	$-v_1/2$	$-v_2/2$	$-v_2/2$	$v_2/2$	$-v_1/6-v_2/6$	$v_1/3+v_2/3$
1	0	1	0	0	1	$v_1/2$	$-v_1/2$	$v_1/2$	$-v_2/2$	$-v_2/2$	$v_2/2$	$-v_1/6-v_2/6$	$v_1/3+v_2/3$
1	0	0	0	0	1	$v_1/2$	$-v_1/2$	$-v_1/2$	$-v_2/2$	$-v_2/2$	$v_2/2$	$v_1/6-v_2/6$	$2v_1/3+v_2/3$
0	1	1	0	0	1	$-v_1/2$	$v_1/2$	$v_1/2$	$-v_2/2$	$-v_2/2$	$v_2/2$	$-v_1/6-v_2/6$	$-2v_1/3+v_2/3$
0	1	0	0	0	1	$-v_1/2$	$v_1/2$	$-v_1/2$	$-v_2/2$	$-v_2/2$	$v_2/2$	$v_1/6-v_2/6$	$-v_1/3+v_2/3$
0	0	1	0	0	1	$-v_1/2$	$-v_1/2$	$v_1/2$	$-v_2/2$	$-v_2/2$	$v_2/2$	$v_1/6-v_2/6$	$-v_1/3+v_2/3$
0	0	0	0	0	1	$-v_1/2$	$-v_1/2$	$-v_1/2$	$-v_2/2$	$-v_2/2$	$v_2/2$	$v_1/2-v_2/6$	$v_2/3$
1	1	1	0	1	0	$v_1/2$	$v_1/2$	$v_1/2$	$-v_2/2$	$v_2/2$	$-v_2/2$	$-v_1/2-v_2/6$	$v_2/3$
1	1	0	0	1	0	$v_1/2$	$v_1/2$	$-v_1/2$	$-v_2/2$	$v_2/2$	$-v_2/2$	$-v_1/6-v_2/6$	$v_1/3+v_2/3$
1	0	1	0	1	0	$v_1/2$	$-v_1/2$	$v_1/2$	$-v_2/2$	$v_2/2$	$-v_2/2$	$-v_1/6-v_2/6$	$v_1/3+v_2/3$
1	0	0	0	1	0	$v_1/2$	$-v_1/2$	$-v_1/2$	$-v_2/2$	$v_2/2$	$-v_2/2$	$v_1/6-v_2/6$	$2v_1/3+v_2/3$
0	1	1	0	1	0	$-v_1/2$	$v_1/2$	$v_1/2$	$-v_2/2$	$v_2/2$	$-v_2/2$	$-v_1/6-v_2/6$	$-2v_1/3+v_2/3$
0	1	0	0	1	0	$-v_1/2$	$v_1/2$	$-v_1/2$	$-v_2/2$	$v_2/2$	$-v_2/2$	$v_1/6-v_2/6$	$-v_1/3+v_2/3$
0	0	1	0	1	0	$-v_1/2$	$-v_1/2$	$v_1/2$	$-v_2/2$	$v_2/2$	$-v_2/2$	$v_1/6-v_2/6$	$-v_1/3+v_2/3$
0	0	0	0	1	0	$-v_1/2$	$-v_1/2$	$-v_1/2$	$-v_2/2$	$v_2/2$	$-v_2/2$	$v_1/2-v_2/6$	$v_2/3$
1	1	1	0	1	1	$v_1/2$	$v_1/2$	$v_1/2$	$-v_2/2$	$v_2/2$	$v_2/2$	$-v_1/2+v_2/6$	$2v_2/3$
1	1	0	0	1	1	$v_1/2$	$v_1/2$	$-v_1/2$	$-v_2/2$	$v_2/2$	$v_2/2$	$-v_1/6+v_2/6$	$v_1/3+2v_2/3$
1	0	1	0	1	1	$v_1/2$	$-v_1/2$	$v_1/2$	$-v_2/2$	$v_2/2$	$v_2/2$	$-v_1/6+v_2/6$	$v_1/3+2v_2/3$
1	0	0	0	1	1	$v_1/2$	$-v_1/2$	$-v_1/2$	$-v_2/2$	$v_2/2$	$v_2/2$	$v_1/6+v_2/6$	$2v_1/3+2v_2/3$
0	1	1	0	1	1	$-v_1/2$	$v_1/2$	$v_1/2$	$-v_2/2$	$v_2/2$	$v_2/2$	$-v_1/6+v_2/6$	$-2v_1/3+2v_2/3$
0	1	0	0	1	1	$-v_1/2$	$v_1/2$	$-v_1/2$	$-v_2/2$	$v_2/2$	$v_2/2$	$v_1/6+v_2/6$	$-v_1/3+2v_2/3$
0	0	1	0	1	1	$-v_1/2$	$-v_1/2$	$v_1/2$	$-v_2/2$	$v_2/2$	$v_2/2$	$v_1/6+v_2/6$	$-v_1/3+2v_2/3$
0	0	0	0	1	1	$-v_1/2$	$-v_1/2$	$-v_1/2$	$-v_2/2$	$v_2/2$	$v_2/2$	$v_1/6+v_2/6$	$2v_2/3$

mid-stage fundamental frequency is intentionally chosen relatively high in order to reduce the value of the three-phase inductors and the size of the magnetic core.

The simulation results are presented in Figs. 6 and 7. Fig. 6 illustrates the system response during start-up, whereas Fig. 7 shows the steady-state waveforms of the mid-stage currents and DC load voltage. The system operates with a regulated voltage at the DC output stage. The currents are all in phase with their corresponding AC-side source voltages, and their total harmonic distortion is $<1\%$.

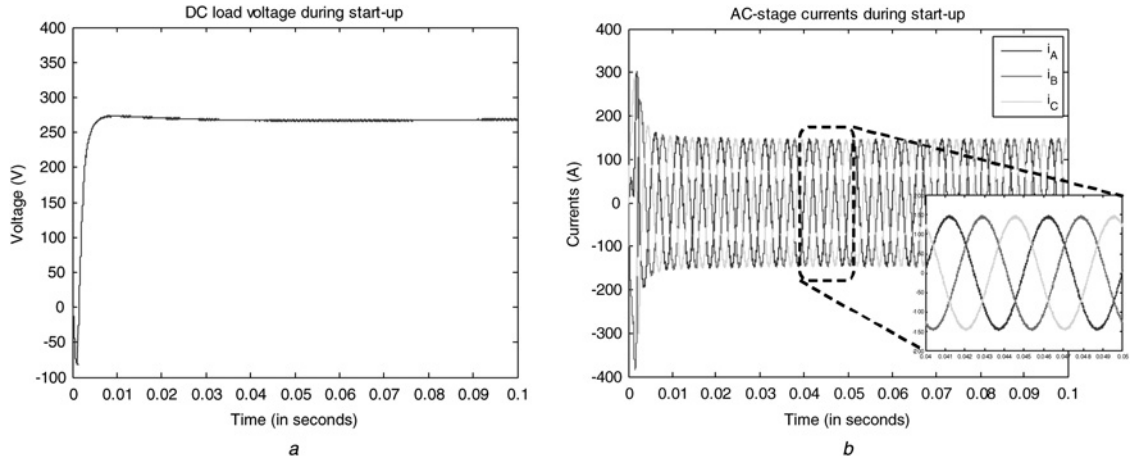


Fig. 6 *Simulation results: waveforms of*

a DC load voltage v_2
b AC-stage currents i_A, i_B and i_C during start-up

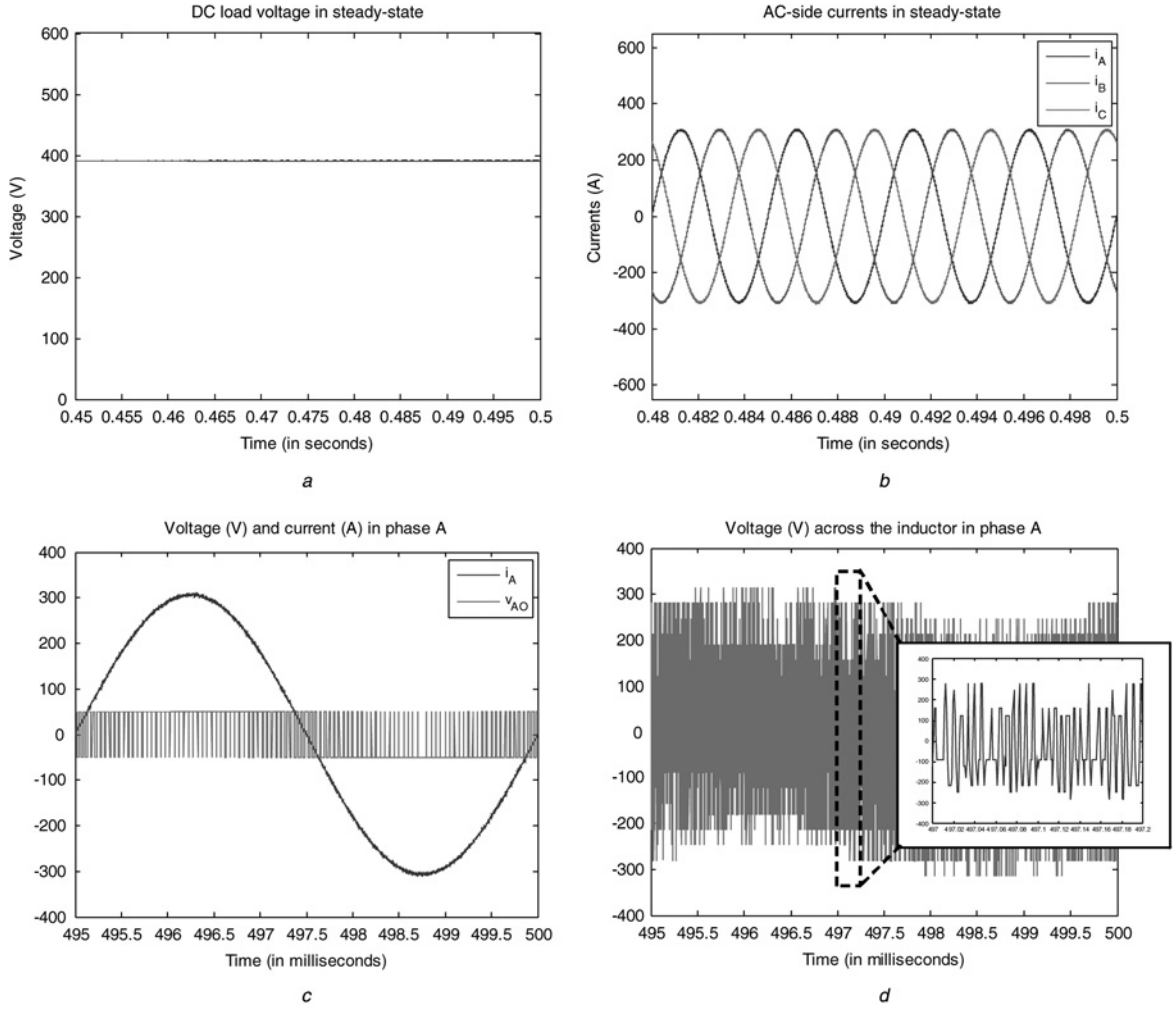


Fig. 7 *Simulation results: steady-state waveforms of*

a DC load voltage v_2
b AC-stage currents i_A, i_B and i_C
c Current i_A and voltage v_{AO} in phase A
d Voltage $v_{AA'}$ across the inductor in phase A

doi: 10.1049/iet-pel.2010.0210

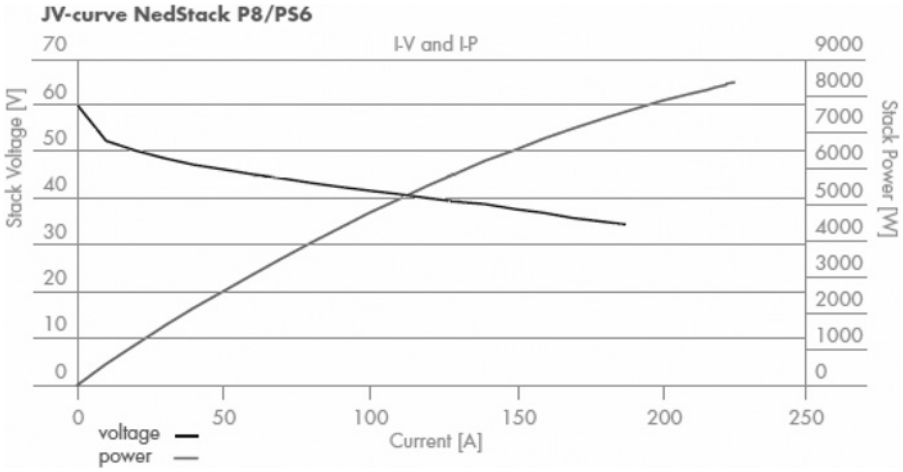


Fig. 8 *I–V and I–P curves of a NedStack PS6 PEMFC*

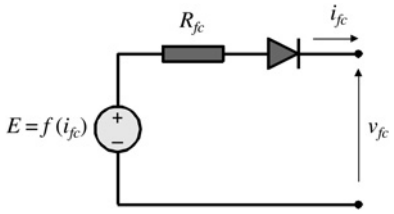


Fig. 9 *PEMFC stack model*

5.2 Case of a PEMFC DC source

A 6 kW-45 V PEMFC stack from NedStack (NedStack PS6) is then chosen as the DC source of energy. The corresponding current–voltage and current–power curves are given in Fig. 8 [10]. Based on the work presented in [11], a PEMFC stack can be modelled as illustrated in Fig. 9. The stack output

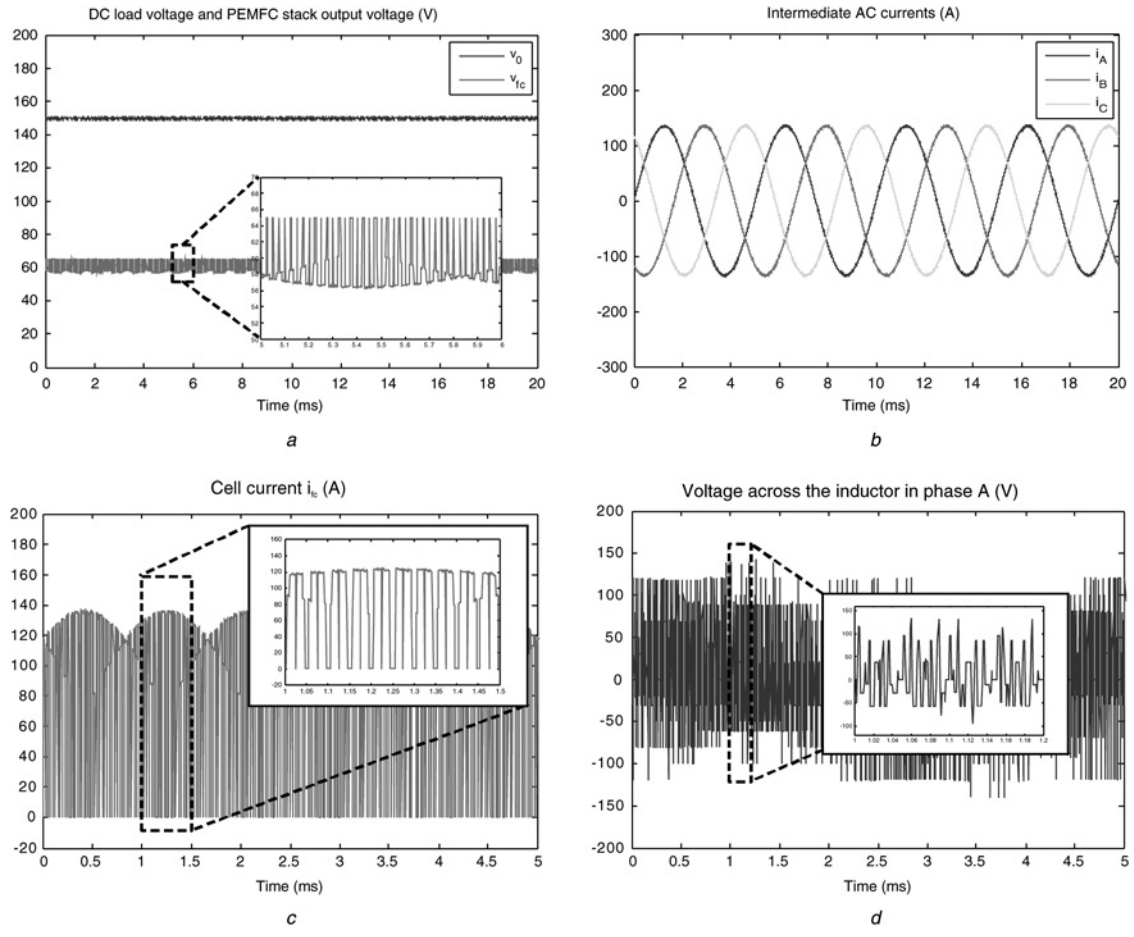
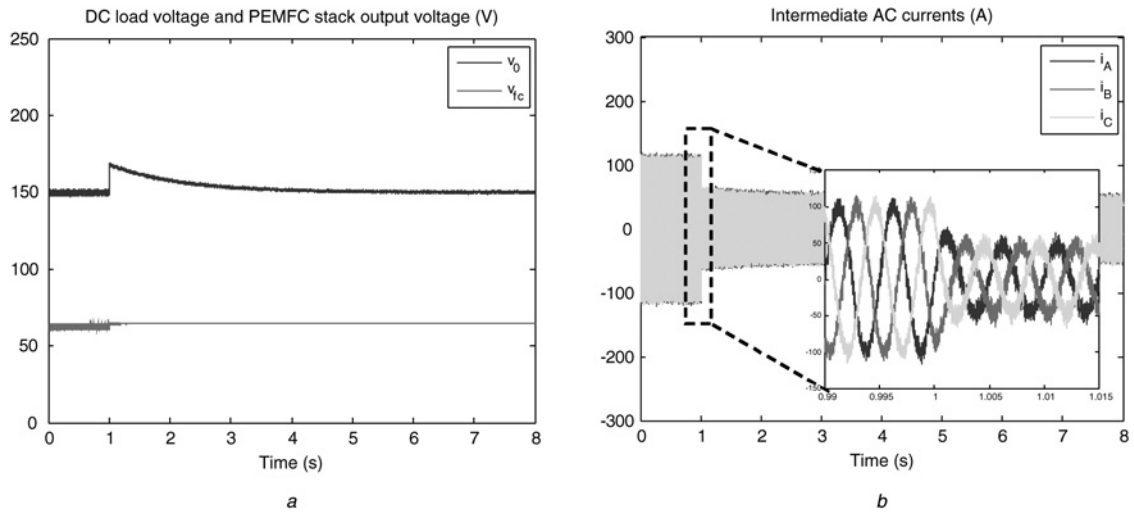


Fig. 10 *Steady-state waveforms at full load of*

a DC load voltage and the PEMFC stack output voltage
b AC mid-stage currents
c Cell current
d Voltage across the inductor in phase A

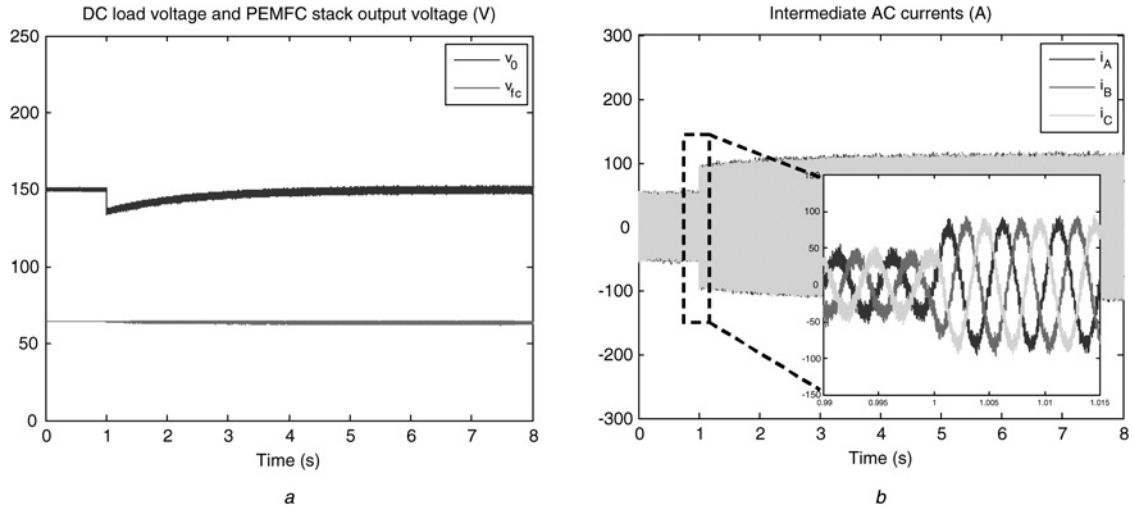


a

b

Fig. 11 *Impacts of a load step decrease (from 6 to 3 kW) on*

a DC load voltage and the PEMFC stack output voltage
b AC mid-stage currents

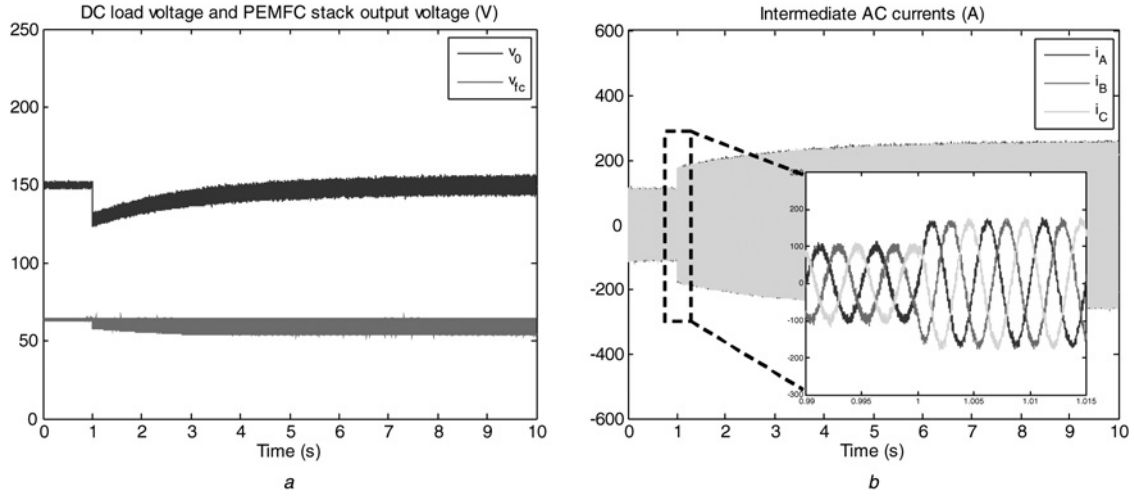


a

b

Fig. 12 *Impacts of a load step increase (from 3 to 6 kW) on*

a DC load voltage and the PEMFC stack output voltage
b AC mid-stage currents



a

b

Fig. 13 *Impacts of a load step increase (from 6 to 12 kW) on*

a DC load voltage and the PEMFC stack output voltage
b AC mid-stage currents

doi: 10.1049/iet-pel.2010.0210

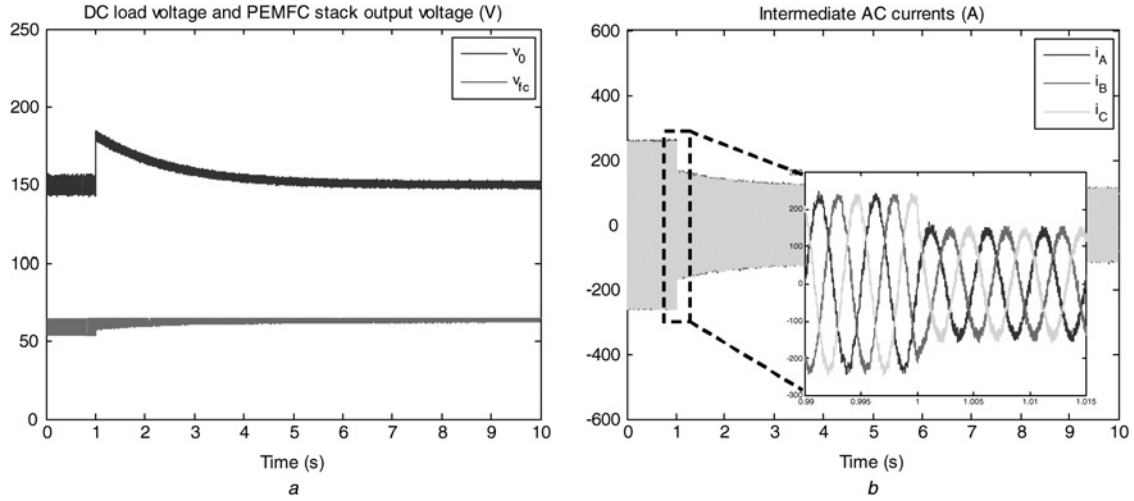


Fig. 14 *Impacts of a load step decrease (from 12 to 6 kW) on*

a DC load voltage and the PEMFC stack output voltage
b AC mid-stage currents

voltage v_{fc} is expressed in terms of the cell current i_{fc} and the stack parameters as follows

$$v_{fc} = E - R_{fc} i_{fc} = E_{\text{oc}} - NA \ln\left(\frac{i_{fc}}{i_0}\right) \cdot \frac{1}{T_d s + 1} - R_{fc} i_{fc} \quad (60)$$

$$E_{\text{oc}} = NE_n \quad (61)$$

where R_{fc} denotes the stack resistance, E_{oc} the open circuit voltage, N the number of cells in series, E_n the Nernst voltage, A the Tafel slope, i_0 the exchange current and T_d the fuel cell response time.

The numerical values of the PEMFC parameters are given in the Appendix 2. The operating set point is chosen as follows:

Desired DC load voltage $v_2^* = 150$ V;
rated load power $P = 6$ kW.

The simulation results showing the system performance in the steady-state at full load are presented in Fig. 10. The system operates with a regulated voltage at the DC output stage and a nearly unity power factor at the AC mid-stage. The total harmonic distortion of the mid-stage currents is $<1\%$. Figs. 11 and 12 show the system's response to load step changes in the under-load range, whereas Figs. 13 and 14 present the system's response to load step changes in the over-load region. In all cases, the load steps are applied at $t = 1$ s, and the obtained system response time is ~ 4 s.

6 Conclusion

In this paper, a two-stage DC–DC converter for high current applications has been analysed. A state-space model of the converter has been developed using the switching functions approach, and a multiple-loop control scheme was designed for the output stage rectifier in order to ensure a high power factor at the AC stage, and a regulated voltage at the DC load. The performance of the proposed control system was verified through numerical simulations, where an ideal DC source and a PEMFC DC source have been considered consecutively. It was shown that, in both cases, the converter exhibits high operation quality in term of mid-stage current distortion and power factor.

7 Acknowledgment

The authors gratefully thank Canada Research Chair in Energy Conversion and Power Electronics for their financial support.

8 References

1 Zhang, J.M., Zhang, F., Xie, X.G., Jiao, D.Z., Zhaoming, Q.: 'A novel ZVS DC/DC converter for high power applications'. Seventeenth Annual IEEE Applied Power Electronics Conf. and Exposition (APEC'02), 10–14 March 2002, vol. 2, pp. 635–640
2 Xiaobo, Y., Xiaofeng, S., Weiyang, W.: 'A novel bidirectional three phase boost DC/DC converter as front-end stage for high power applications'. Thirty-Seventh Annual IEEE Power Electronics Specialist Conf. (PESC'06), 18–22 June 2006, pp. 1–5
3 Hanju, C., Enjeti, P.: 'A novel three-phase high power current-fed DC/DC converter with active clamp for fuel cells'. Thirty-Eighth Annual IEEE Power Electronics Specialist Conf. (PESC'07), 17–21 June 2007, pp. 2485–2489
4 Oliveira, D.S., Barbi, I.: 'A three-phase ZVS PWM DC/DC converter with asymmetrical duty cycle for high power applications'. Thirty-Fourth Annual IEEE Power Electronics Specialist Conf. (PESC'03), 15–19 June 2003, vol. 2, pp. 616–621
5 Jacobs, J., Averberg, A., De Doncker, R.: 'A novel three-phase DC/DC converter for high-power applications'. Thirty-Fifth Annual IEEE Power Electronics Specialist Conf. (PESC'04), Aachen, Germany, 2004, pp. 1861–1867
6 Wu, R., Dewan, S.B., Slemon, G.R.: 'Analysis of an AC-to-DC voltage source converter using PWM with phase and amplitude control', *IEEE Trans. Ind. Appl.*, 1991, **27**, (2), pp. 355–364
7 Kanaan, H.Y., Al-Haddad, K.: 'A comparison between three modeling approaches for computer implementation of high-fixed-switching-frequency power converters operating in a continuous mode'. Proc. CCECE'02, Winnipeg, Manitoba, Canada, 12–15 May 2002, vol. 1, pp. 274–279
8 Kanaan, H.Y., Al-Haddad, K.: 'Switching-functions-based modeling of a three-phase three-switch three-level rectifier in continuous and discontinuous modes for real-time simulations'. Proc. 27th Int. Telecommunication Energy Conf. (INTELEC'05), Berlin, Germany, 18–22 September 2005
9 Maciejowski, J.M.: 'Multivariable feedback design' (Addison-Wesley, 1989)

10 www.fuelcellmarkets.com/content/images/articles/ps6.pdf
11 Njoya Motapon, S.: 'A generic fuel cell model and experimental validation'. Ecole de Technologie Supérieure, Département de Génie Electrique, Mémoire de Maîtrise, Montréal, Canada, June 2008

9 Appendix 1: DC–DC converter and control system parameters

Fundamental frequency $f = \omega/2\pi = 200$ Hz;
Switching frequency $f_S = 20$ kHz;
AC-side inductors $L = 100$ μH, each;
DC-side capacitor $C_2 = 1$ mF;
Feedback scaling gains $K_i = K_v = 1$;
Inner regulators $H_{i,d}(s) = H_{i,q}(s) = -(s + 45)/s$;
Outer regulator $H_v(s) = 3(s + 1)/s$.

10 Appendix 2: PEMFC parameters

Open circuit voltage $E_{oc} = 65$ V;
Number of cells in series $N = 65$;
Nernst voltage $E_n = 1$ V;
Tafel slope $A = 30.7$ mV;
Exchange current $i_0 = 0.94$ A;
Fuel cell response time $T_d = 10$ s;
Stack resistance $R_{fc} = 75.8$ mΩ.

doi: 10.1049/iet-pel.2010.0210