Voltage Gain Enhancement for Step-Up Converter Constructed by KY and Buck-Boost Converters

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***Abstract*—In this paper, a novel voltage-boosting converter is presented, which combines one charge pump and one coupled inductor with the turns ratio. The corresponding voltage gain is greater than that of the existing step-up converter combining KY and buck-boost converters. Since the proposed converter possesses an output inductor, the output current is non-pulsating. After some mathematical deductions, an experimental set-up with 12V input voltage, 72V output voltage, and 60W output power is used to verify the effectiveness of the proposed converter.**

***Keywords*—KY converter, charge pump, coupled inductor.**

I. Introduction

Because of the global warming, the demand of the green power has been increasing for decades. These kinds of green power facilities include solar cells, fuel cells, etc. In many applications, high voltage conversion converters play an important role in boosting the low output voltages of green power facilities to the high voltages which the loads need. Regarding the traditional non-isolated voltage-boosting converters [1], [2], such as the traditional boost converter and buck-boost converter, their voltage gains are not high enough. Up to now, many kinds of voltage-boosting techniques have been presented, including several inductors which are magnetized and then pump the stored energy into the output with all inductors connected in series [3], coupled inductors with turns ratios [4]-[8], [10], [11], [15], voltage superposition based on switching capacitors [9], [13]-[18], auxiliary transformers with turns ratios [12], etc. In [8] and [10], the output terminal is floating, thereby increasing application complexity. In [4]-[11], [16] and [17] these converters contain too many components, thereby making the converters relatively complicated. In [3]-[11], [15], [16] and [17], the output currents are pulsating, therefore causing the output voltage ripples to tend to be large. In [12], [13], [14] and [18] even though the output currents are non-pulsating, their voltage gains are not high enough. As described in the appendix, Table III makes a comparison between the converters shown in the references, in terms of voltage gain, component number, switch voltage stress, output inductor and floating output.

Based on the mentioned above, a novel step-up converter is presented. This converter combines one KY converter [12], one traditional synchronously rectified (SR) buck-boost converter, and one coupled inductor with the turns ratio, which is used to improve the voltage gain. Therefore, the voltage gain is higher than that of the converter in [14] and can be determined by adjusting both the duty cycle and the turns ratio. Besides, the duty cycle and the turns ratio are independent, which means that tuning the duty cycle does not affect the turns ratio and vice versa. In addition, the proposed step-up converter has no floating output, and has an output inductor so the output current is non-pulsating. Furthermore, part of the leakage inductance energy can be recycled to the output capacitor of the SR buck-boost converter. In this paper, a detailed description along with some experimental results is given to provide the effectiveness of the proposed converter.

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II. Overall System Configuration

Fig. 1 shows the proposed converter, which contains two MOSFET switches S_1 and S_2, one coupled inductor composed of the primary winding with N_p turns and the secondary winding with N_s turns, one energy-transferring capacitor C_1, one charge pump capacitor C_2, one diode D_1, one output inductor L_o, and one output capacitor C_o. In addition, the input voltage is denoted by V_i, the output voltage is signified by V_o, and the output resistor is represented by R_o.

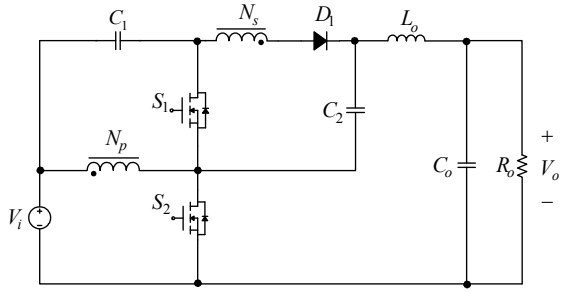

Fig. 1. Proposed step-up converter.

III. Basic Operating Principles

Before taking up this section, there are some assumptions to be made as follows.

(1) The coupled inductor is modeled as an ideal transformer except that one magnetizing inductor L_m is connected in parallel with the primary winding and one leakage inductor L_{l1} is connected in series with the primary winding. Therefore, the coupling coefficient k is defined as $L_m/(L_m + L_{l1})$.

(2) The proposed converter operates in the positive current mode. That is, the currents flowing through the magnetizing inductor L_m and the output inductor L_o are always positive.

(3) The dead times between the two MOSFET switches are omitted.

(4) The MOSFET switches and the diodes are assumed to be ideal components.
(5) The values of all the capacitors are large enough such that the voltages across them are kept constant at some values.
(6) The magnitude of the switching ripple is negligible. Therefore, the small ripple approximation will be adopted herein in analysis.

The following analysis contains the explanation of the power flow path for each mode, along with the corresponding equations and voltage gain. Inherently, there are two operating modes in the proposed converter. And, the gate driving signals v_{gs1} and v_{gs2} of the two switches S_1 and S_2 have the duty cycles of $(1-D)$ and D, respectively, where D is the dc quiescent duty cycle created from the controller. In addition, the input current is denoted by i_i, the current through the N_p winding is signified by i_{Np}, the current through the N_s winding is represented by i_{Ns}, the current through L_m is denoted by i_{Lm}, the current through L_o is indicated by i_{Lo}, and the current through R_o is signified by I_o. On the other hand, the voltage across L_m or the voltage across the N_p winding is signified by v_{Np}, the voltage across the N_s winding is represented by v_{Ns}, the voltage across C_1 is indicated by V_{C1}, the voltage across C_2 is denoted by V_{C2}, and the voltage across L_o is described by v_{Lo}.

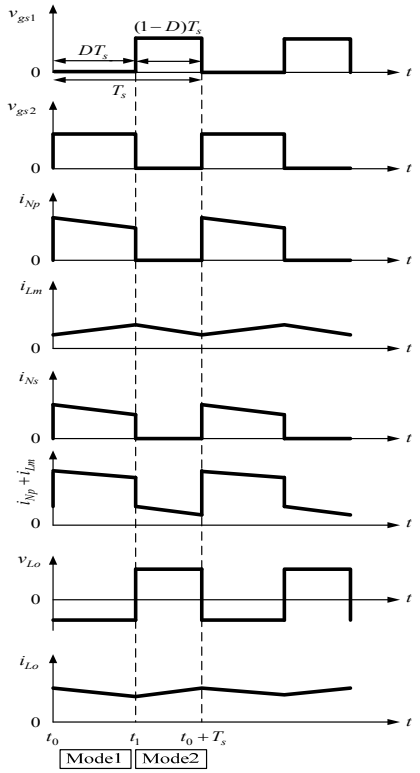

Fig. 2. Key waveforms of the proposed converter.

A. *Voltage Gain Considering Coupling Coefficient Equal to One*

In this case, the coupling coefficient k is equal to one, that is, the leakage inductor is omitted. Besides, the key waveforms of the proposed converter with two operating modes are shown in Fig. 2.

1) Mode 1: During this interval, as shown in Fig. 3, S_1 is turned off, but S_2 is turned on. Therefore, the input voltage V_i is imposed on N_p, thus causing L_m to be magnetized and the voltage across N_s to be induced, equal to $V_i \times N_s / N_p$. In addition, D_1 becomes forward-biased, C_2 is charged to $V_i + V_{C1} + V_i \times N_s / N_p$, and the voltage across L_o, v_{Lo}, is a negative value, equal to $V_{C2} - V_o$, thus making L_o demagnetized. As a consequence, the input voltage V_i, together with the voltage across C_1, V_{C1}, plus the induced voltage on N_s, v_{Ns}, plus the voltage across L_o, v_{Lo}, provides the energy to the load. Also, the associated equations are shown below:

$$v_{Np} = V_i \tag{1}$$

$$v_{Lo} = V_{C2} - V_o \tag{2}$$

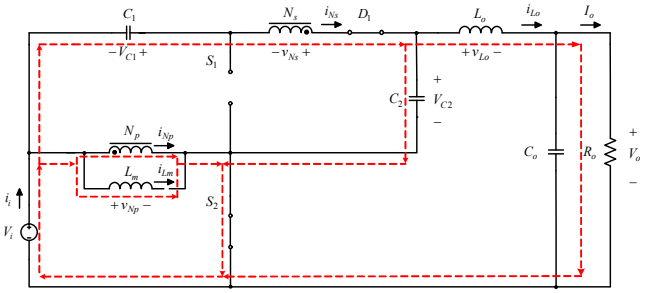

Fig. 3. Power flow in mode 1 with coupling coefficient equal to one.

2) Mode 2: During this interval, as shown in Fig. 4, S_1 is turned on, but S_2 is turned off. Therefore, the voltage $-V_{C1}$ is imposed on N_p, thereby causing the magnetizing inductor L_m to be demagnetized, and the voltage across N_s to be induced, equal to $-V_{C1} \times N_s / N_p$. In addition, D_1 becomes reverse-biased, the voltage on L_o is a positive value, equal to $V_i + V_{C1} + V_{C2} - V_o$, thus causing L_o to be magnetized. As a result, the input voltage V_i, together with the voltage across L_m, v_{Np}, plus the voltage across C_2, V_{C2}, provides the energy to L_o and the load. Also, the corresponding equations are shown below:

$$v_{Np} = -V_{C1} \tag{3}$$

$$v_{Lo} = V_i + V_{C1} + V_{C2} - V_o \tag{4}$$

By applying the voltage-second balance principle to L_m over one switching period, the following equation can be obtained:

$$V_i \times D + (-V_{C1}) \times (1-D) = 0 \tag{5}$$

Also, by rearranging the above equation, the voltage across C_1, V_{C1}, can be obtained as follows:

$$V_{C1} = \frac{D}{1-D} \times V_i \tag{6}$$

Likewise, by applying the voltage-second balance principle to L_o over one switching period, the following equation can be obtained:

$$(V_{C2}-V_o)\times D+(V_i+V_{C1}+V_{C2}-V_o)\times(1-D)=0 \quad (7)$$

The voltage across C_2, V_{C2}, can be represented by

$$V_{C2}=V_i+V_{C1}+V_i\times\frac{N_s}{N_p} \quad (8)$$

Next, based on (6), (7) and (8), the corresponding voltage gain can be expressed to be

$$\frac{V_o}{V_i}=\frac{2-D}{1-D}+\frac{N_s}{N_p} \quad (9)$$

From (9), it can be seen that $0<D<1$.

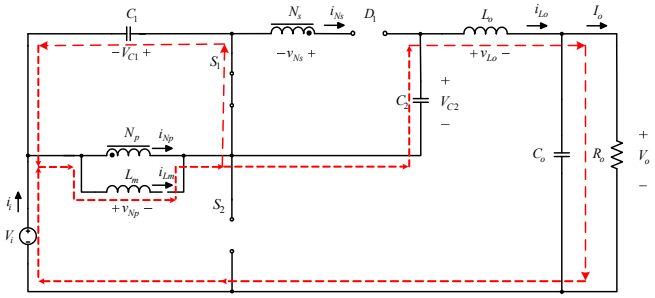

Fig. 4. Power flow in mode 2 with coupling coefficient equal to one.

B. Voltage Gain Considering Coupling Coefficient Not Equal to One

In this case, the coupling coefficient k is not equal to one, that is, the leakage inductor L_{l1} is taken into account. Moreover, the operating modes are also the same as those mentioned in section III.A.

1) Mode 1: During this interval, as shown in Fig. 5, the following equations, containing the coupling coefficient k, can be obtained. At the same time, both L_m and L_{l1} are magnetized simultaneously. Hence, the corresponding equations are shown below:

$$v_{Np}=\frac{L_m}{L_m+L_{l1}}\times V_i=kV_i \quad (10)$$

$$v_{Ns}=v_{Np}\times\frac{N_s}{N_p}=kV_i\times\frac{N_s}{N_p} \quad (11)$$

In addition, the voltages on C_2 and L_o can be depicted as follows:

$$V_{C2}=V_i+V_{C1}+v_{Ns}=V_i+V_{C1}+kV_i\times\frac{N_s}{N_p} \quad (12)$$

$$v_{Lo}=V_{C2}-V_o \quad (13)$$

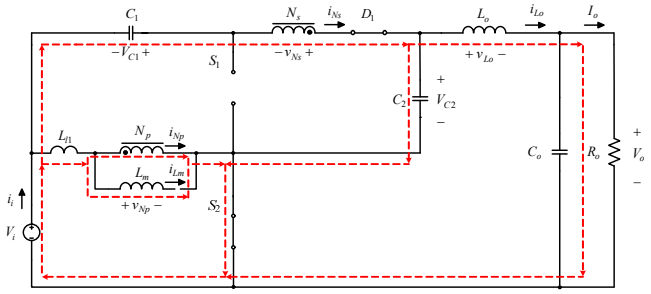

Fig. 5. Power flow in mode 1 with coupling coefficient smaller than one.

2) Mode 2: During this interval, as shown in Fig. 6, the voltages across L_o and C_1 is to be expressed as follows. Above all, part of the energy stored in L_m and L_{l1} can be transferred to C_1. Hence, the corresponding equations are shown below:

$$v_{Np}=-kV_{C1} \quad (14)$$

$$v_{Lo}=V_i+V_{C1}+V_{C2}-V_o \quad (15)$$

By applying the voltage-second balance to both L_m and L_{l1} over one switching period, one can get

$$V_i\times D+(-V_{C1})\times(1-D)=0 \quad (16)$$

Sequentially, by rearranging the above equation, the voltage across C_1, V_{C1}, can be obtained to be

$$V_{C1}=\frac{D}{1-D}\times V_i \quad (17)$$

Likewise, by applying the voltage-second balance principle to L_o over one switching period, the following equation can be obtained to be

$$(V_{C2}-V_o)\times D+(V_i+V_{C1}+V_{C2}-V_o)\times(1-D)=0 \quad (18)$$

Next, substituting (12) and (17) into (18) yields the voltage gain:

$$\frac{V_o}{V_i}=\frac{2-D}{1-D}+k\frac{N_s}{N_p} \quad (19)$$

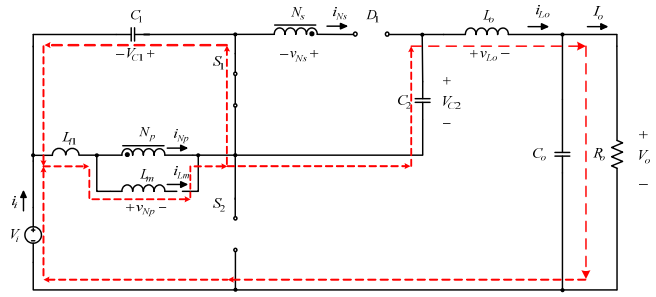

Fig. 6. Power flow in mode 2.

Fig. 7 shows the curves of voltage gain versus duty cycle of the proposed converter, considering different values of coupling coefficient k with the same turns ratio n ($=N_s/N_p$) set to three. Fig. 8 depicts the curves of voltage gain versus duty cycle of the proposed converter, considering different turns ratios with the same coupling coefficient set to one. Fig. 9 illustrates the voltage gain of the proposed converter versus duty cycle of the proposed converter without any negative

magnetizing inductor current and any negative output inductor current, as compared with the traditional boost converter in [1] and the converter in [14].

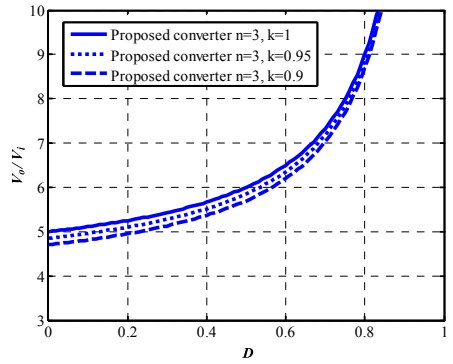

Fig. 7. Curves of voltage gain versus duty cycle for the proposed converter with different values of coupling coefficient k but the same turns ratio n.

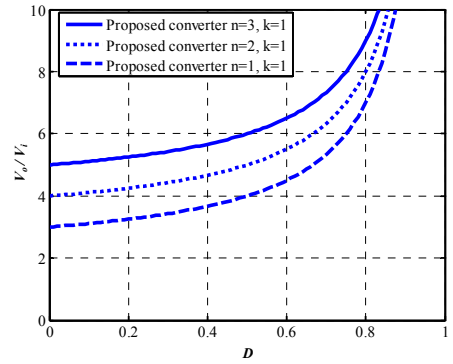

Fig. 8. Curves of voltage gain versus duty cycle for the proposed converter with different values of turns ratio n but the same coupling coefficient k.

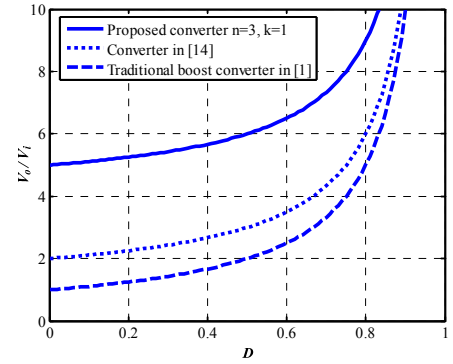

Fig. 9. Comparison of voltage gain versus duty cycle for three types of converters.

C. Boundary Condition for Magnetizing Inductor

The condition for the magnetizing inductor L_m operating in what region will be described as follows:

$$\begin{cases} 2I_{Lm} \geq \Delta i_{Lm}, \text{for all current values in the positive current region} \\ 2I_{Lm} < \Delta i_{Lm}, \text{for part of current values in the negative current region} \end{cases} \quad (20)$$

where I_{Lm} and Δi_{Lm} are the dc and ac components of i_{Lm}, respectively.

The expression of I_{Lm} can be obtained from (21) to (24). For analysis convenience, it is assumed that the input power is equal to the output power. According to the voltage-second balance for the inductor and the ampere-second balance for the capacitor, the dc component of the inductor voltage and the dc component of the capacitor current are zero. Therefore, as shown in Fig. 10, from the dc component of i_{Ns}, I_{Ns}, is equal to the output current I_o; likewise, as shown in Figs. 10 and 11, the current I_i, entering into the primary side of the coupled inductor, is the dc component of i_i, and is equal to the dc component of i_{Np}, I_{Np}, plus the dc component of i_{Lm}, I_{Lm}. Therefore,

$$I_i = \left(\frac{2-D}{1-D} + \frac{N_s}{N_p}\right) \times I_o \quad (21)$$

$$I_{Np} = \frac{N_s}{N_p} \times I_{Ns} = \frac{N_s}{N_p} \times I_o \quad (22)$$

$$I_{Lm} = I_i - I_{Np} = \frac{2-D}{1-D} \times I_o \quad (23)$$

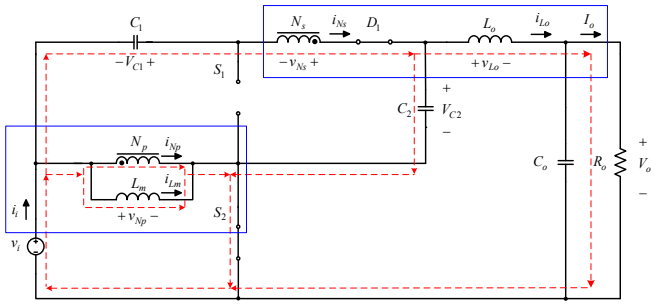

Fig. 10. Marked area in the proposed converter used to explain I_{Np} and I_{Lm}.

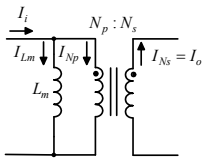

Fig. 11. Equivalent model for the dc analysis of the coupled inductor.

In Fig. 11, I_o can be expressed as V_o/R_o. Substituting V_o/R_o for I_o in (23) yields the following equation:

$$I_{Lm} = \frac{2-D}{1-D} \times \frac{V_o}{R_o} \quad (24)$$

Also, Δi_{Lm} can be represented by

$$\Delta i_{Lm} = \frac{v_{Np}\Delta t}{L_m} = \frac{V_i D T_s}{L_m} \quad (25)$$

As $2I_{Lm} \geq \Delta i_{Lm}$, L_m operates in the positive current region. Moreover, the further deduction is shown as follows:

$$2I_{Lm} \geq \Delta i_{Lm}$$

$$\Rightarrow 2 \times \left(\frac{2-D}{1-D} \times \frac{V_o}{R_o}\right) \geq \frac{V_i D T_s}{L_m}$$

$$\Rightarrow \frac{2L_m}{R_o T_s} \geq \frac{D(1-D)^2}{(2+n-D-nD)(2-D)} \quad (26)$$

$$\Rightarrow K_1 \geq K_{crit1}(D)$$

where $K_1 = \dfrac{2L_m}{R_o T_s}$ and $K_{crit1}(D) = \dfrac{D(1-D)^2}{(2+n-D-nD)(2-D)}$.

From (26), the relationship between $K_{crit1}(D)$ and D is shown in Fig. 12 under the condition that n is set at three. From Fig. 12, it can be seen that if $K_{crit1}(D)$ is larger than K_1, L_m will operate in the positive current region; otherwise, part of i_{Lm} will enter into the negative current region.

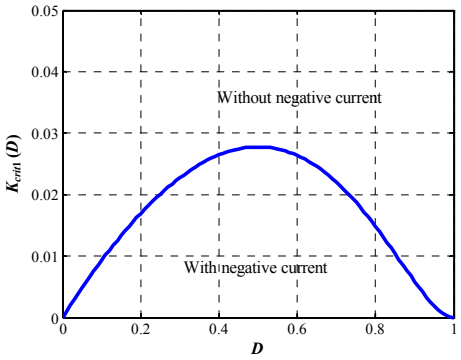

Fig. 12. Boundary condition for magnetizing inductor L_m.

D. Boundary Condition for Output Inductor

The conditions for the output inductor L_o operating in what region will be described as follows:

$$\begin{cases} 2I_{Lo} \geq \Delta i_{Lo}, \text{for all current values in the positive current region} \\ 2I_{Lo} < \Delta i_{Lo}, \text{for part of current values in the negative current region} \end{cases} \quad (27)$$

where I_{Lo} and Δi_{Lo} are the dc and ac components of i_{Lo}, respectively.

Since I_{Lo} is equal to I_o, replacing I_o with V_o/R_o yields the following equation:

$$I_{Lo} = \frac{V_o}{R_o} \quad (28)$$

Also, Δi_{Lo} can be expressed by

$$\Delta i_{Lo} = \frac{v_{Lo}\Delta t}{L_o} = \frac{(V_i + V_{C1} + V_{C2} - V_o) \times (1-D)T_s}{L_o} \quad (29)$$

Inserting equations (4), (6) and (7) into (29) yields the following equation:

$$\Delta i_{Lo} = \frac{V_i D T_s}{L_o} \quad (30)$$

As $2I_{Lo} \geq \Delta i_{Lo}$, L_o operates in the positive current region. In addition, the more deduction is shown as following:

$$\begin{aligned} & 2I_{Lo} \geq \Delta i_{Lo} \\ \Rightarrow & 2 \times \frac{V_o}{R_o} \geq \frac{V_i D T_s}{L_o} \\ \Rightarrow & \frac{2L_o}{R_o T_s} \geq \frac{D(1-D)}{2+n-D-nD} \\ \Rightarrow & K_2 \geq K_{crit2}(D) \end{aligned} \quad (31)$$

where $K_2 = \dfrac{2L_o}{R_o T_s}$ and $K_{crit2}(D) = \dfrac{D(1-D)}{2+n-D-nD}$.

From (31), the relationship between $K_{crit2}(D)$ and D is shown in Fig. 13. From Fig. 13, it can be seen that if $K_{crit2}(D)$ is larger than K_2, L_o will operate in the positive current region; otherwise, part of i_{Lo} will enter into the negative current region.

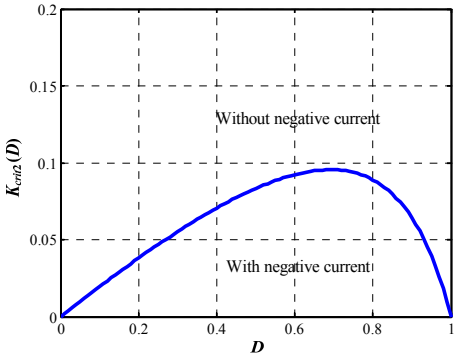

Fig. 13. Boundary condition for output inductor L_o.

IV. Control Method Applied with Design Considerations

Fig. 14 shows the overall system block diagram. First of all, the voltage divider transfers the output voltage to a desired lower value, which is fed to the analog-to-digital converter (ADC) to create a corresponding digital signal. After this, this digital signal is sent to the filed programmable gate array (FPGA), which is the control kernel, containing one serial peripheral interface (SPI), one proportional-integral (PI) controller, and one digital pulse-width modulation (DPWM) generator. Eventually, the FPGA processes this digital signal, and accordingly produces two gate driving signals to drive the MOSFET switches. The system specifications and used component names of the proposed converter are shown in Tables I and II, respectively. Besides, the PI controller design method is referred to page 95 of the technical report [19]. There are two steps to tune the parameters of the proportional gain k_p and the integral gain k_i in the PI controller as follows.

(1) Step 1: Starting with $k_p \neq 0$ and $k_i = 0$, and trimming k_p until a small residual error is received.

(2) Step 2: Increasing k_i until the system reaches an almost zero final error.

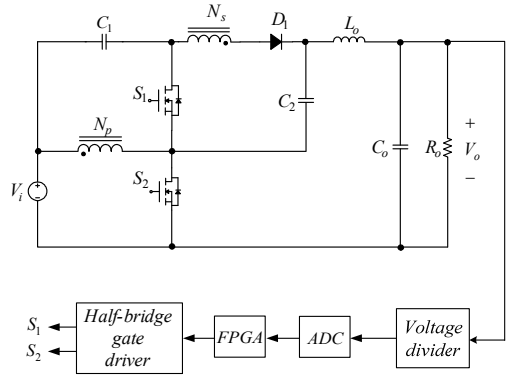

Fig. 14. Proposed overall system block diagram.

Table I System specifications of the proposed converter

System parameters	Specifications
Input voltage (V_i)	12V
Rated output voltage (V_o)	72V
Rated output current ($I_{o,rated}$)/power ($P_{o,rated}$)	0.833A/60W
Minimum output current ($I_{o,min}$)/power ($P_{o,min}$)	0.1A/7.2W
Switching frequency (f_s)	100kHz

Table II Components used in the proposed converter

Components	Specifications
MOSFET switches S_1, S_2	STP120NF, V_{DS}=100V, I_D=120A, R_{on}=10.5mΩ
Diode D_1	V20120C, V_R=120V, $I_{F(AV)}$=20A, V_F=0.54V @ I_F=5A
Energy-transferring capacitor C_1	Two 470μF/50V Rubycon capacitors with positive terminals connected in series
Charge pump capacitor C_2	Two 47μF/100V MIEC capacitors connected in parallel
Output capacitor C_o	Two 220μF/100V MIEC capacitors connected in parallel
Coupled inductor	Core: PTS40/27/I 3C92, N_p:N_s=1:3, L_m=148.7μH, L_{l1}=0.3μH, k≒0.997
Output inductor L_o	Core: ER40/20/13, N=20, air-gap of 0.35mm, L_o=188μH
FPGA	EP1C3T100
Half-bridge gate driver	IR2011
ADC	ADC7476

How to design the magnetizing inductor L_m, the energy-transferring capacitor C_1, the charge pump capacitor C_2, the output capacitor C_o and the output inductor L_o is shown as follows.

A) Inductor Design

1) Magnetizing inductor design: To make sure that L_m always operates in the positive region, the required equation is as follows.

$$L_m \geq \frac{V_i D T_s}{\Delta i_{Lm}} = \frac{V_i D T_s}{2 \times I_{Lm,min}} = \frac{12 \times 0.5 \times 10\mu}{2 \times 0.3} = 100\mu\text{H} \tag{32}$$

where $I_{Lm,min}$ is the minimum dc current in L_m. And finally, the value of L_m is set at 148.7μH.

2) Output inductor design: From the industrial viewpoint, the output inductor is generally designed to have no negative current when the output current is above 20%~30% of the rated output current [20]. Therefore, in this paper, the boundary between the positive current and the negative current is assumed to be at 20% of the rated output current. Hence, the value of L_o can be obtained as follows:

$$\begin{aligned} L_o &= \frac{v_{Lo}\Delta t}{\Delta i_{Lo}} = \frac{(V_i + V_{C1} + V_{C2} - V_o)(1-D)T_s}{\Delta i_{Lo}} \\ &= \frac{(V_i + V_i \times \frac{D}{1-D} + V_i + V_i \times \frac{D}{1-D} + V_i \times \frac{N_s}{N_p} - V_o)(1-D)T_s}{20\% \times I_{o,rated} \times 2} \\ &= \frac{(12 + 12 \times \frac{0.5}{1-0.5} + 12 + 12 \times \frac{0.5}{1-0.5} + 12 \times 3 - 72)(1-0.5) \times 10\mu}{20\% \times \frac{5}{6} \times 2} \\ &= 180\mu\text{H} \end{aligned} \tag{33}$$

Eventually, the value of L_o is set at 188μH.

B) Capacitor Design

1) Energy-transferring capacitor design: Assuming the peak-to-peak value of the capacitor voltage during the charge period, Δv_{C1}, is set to 1% of V_{C1} or less, that is, Δv_{C1} is smaller than 120mV, the value of C_1 can be obtained as follows:

$$\begin{aligned} C_1 &\geq \frac{i_{C1}\Delta t}{\Delta v_{C1}} = \frac{(I_{i,rated} - I_{o,rated})(1-D)T_s}{0.01 \times V_{C1}} \\ \Rightarrow C_1 &\geq \frac{(5 - 0.833)(1-0.5) \times 10\mu}{0.01 \times 12} \approx 174\mu\text{F} \end{aligned} \tag{34}$$

where $I_{i,rated}$ is the dc input current I_i under rated conditions. And eventually, two 470μF capacitors with positive terminals connected in series are selected for C_1 [21].

2) Charge pump capacitor design: Assuming the variation in capacitor voltage during the discharge period, Δv_{C2}, is set to 0.1% of V_{C2} or less, that is, Δv_{C2} is smaller than 60mV, the value of C_2 can be obtained as follows:

$$\begin{aligned} C_2 &\geq \frac{i_{C2}\Delta t}{\Delta v_{C2}} = \frac{I_{Lo,rated}(1-D)T_s}{0.001 \times V_{C2}} = \frac{I_{o,rated}(1-D)T_s}{0.001 \times V_{C2}} \\ \Rightarrow C_2 &\geq \frac{0.833 \times (1-0.5) \times 10\mu}{0.001 \times 60} \approx 69.4\mu\text{F} \end{aligned} \tag{35}$$

where $I_{Lo,rated}$ is the dc current in L_o under rated conditions. And finally, two 47μF capacitors connected in parallel are chosen for C_2 [21].

3) Output capacitor design: As generally known, the output filter is used to filter out the output current ripple as much as possible. Prior to designing C_o, the output voltage ripple Δv_o is assumed to be smaller than 0.1% of the rated output voltage, that is, Δv_o is smaller than 72mV. Therefore, the equivalent series resistance of the output capacitor, *ESR*, can be represented by

$$ESR \leq \frac{\Delta v_o}{\Delta i_{Lo}} = \frac{0.001 \times V_o}{\Delta i_{Lo}} = \frac{0.001 \times 72}{\frac{1}{3}} \approx 0.216\Omega \tag{36}$$

Besides, a rule of thumb for the electrolytic capacitor [2] is

$$C_o \times ESR = 65\mu \quad (37)$$

Therefore, based on (36) and (37), the value of C_o can be represented by

$$C_o \geq \frac{65\mu}{ESR} = \frac{65\mu}{0.216} \approx 300\mu\text{F} \quad (38)$$

Eventually, two 220μF capacitors connected in parallel are selected for C_o [21].

V. Experimental Results

Figs. 15 to 17 show the measured waveforms at light load, namely, I_o=0.1A. Fig. 15 shows the gate driving signal for S_1, v_{gs1}, the gate driving signal for S_2, v_{gs2}, the current passing through the primary side of the coupled inductor, i_{Np}+i_{Lm}, and the current passing through the secondary side of the coupled inductor, i_{Ns}. Fig. 16 shows the gate driving signal for S_1, v_{gs1}, the gate driving signal for S_2, v_{gs2}, the voltage across L_o, v_{Lo}, and the current through L_o, i_{Lo}. Fig. 17 shows the gate driving signal for S_1, v_{gs1}, the gate driving signal for S_2, v_{gs2}, the voltage across C_1, V_{C1}, and the voltage across C_2, V_{C2}. On the other hand, Figs. 18 to 20 show the same measured waveform items as those for Figs. 15 to 17, except for half load, namely, I_o=0.4A, whereas Figs. 21 to 23 show the same waveform items as those for Figs. 15 to 17, except for rated load, namely, I_o=0.833A.

From the waveforms mentioned above, the proposed converter can stably operate all over the load range. Moreover, from Fig. 16, it can be seen that there is a negative current in L_o. Furthermore, the heavier the load is, the higher the voltages across C_1 and C_2. This is because the voltages across C_1 and C_2 are functions of the duty cycle D. That is, as the output current increases, the output voltage will decrease. Therefore, in order to maintain the output voltage at the constant value, the feedback control system will increase D. Consequently, the voltages across C_1 and C_2 will increase as well.

On the other hand, Figs. 24 and 25 show the currents through S_1 and S_2 and the voltages across S_1 and S_2 at rated load. Without the voltage spikes considered, the measured voltage stresses of S_1 and S_2 are both about 27V, which is somewhat different from the idea value of 24V. This is because the voltage drops due to parasitic impedance makes the duty cycle bigger than the ideal value. Without the currents spikes considered, the measured current stresses of S_1 and S_2 are about 3A and 10A, respectively. Furthermore, Figs. 26 and 27 show the waveforms of output voltage and current in the steady state at rated load, and in the transients from light/rated load to rated/light load, respectively. From Fig. 27, it can be seen that the output voltage undershoot due to the load change from light load to rated load is about 4.7V with the corresponding recovery time of about 225ms, whereas the output voltage overshoot due to the load change from rated load to light load is about 4.3V with the resulting recovery time of about 240ms.

Aside from these, Fig. 28 shows the curve of efficiency versus load current. From Fig. 28, it can be seen that the efficiency all over the load range is above 88%, and the maximum efficiency can be up to 95%.

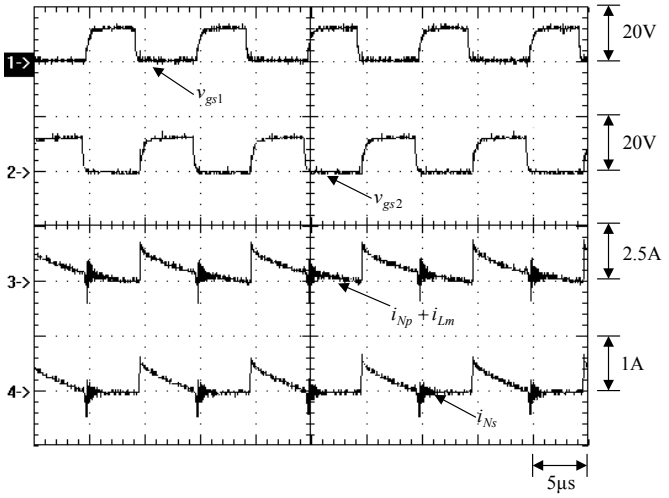

Fig. 15. Waveforms at light load: (1) v_{gs1}; (2) v_{gs2}; (3) i_{Np}+i_{Lm}; (4) i_{Ns}.

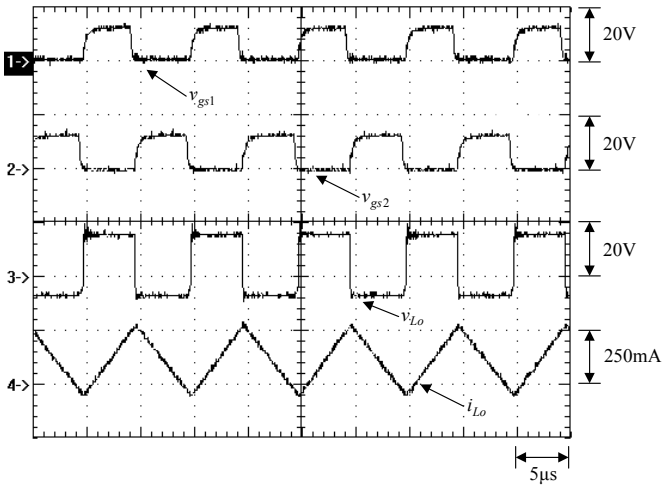

Fig. 16. Waveforms at light load: (1) v_{gs1}; (2) v_{gs2}; (3) v_{Lo}; (4) i_{Lo}.

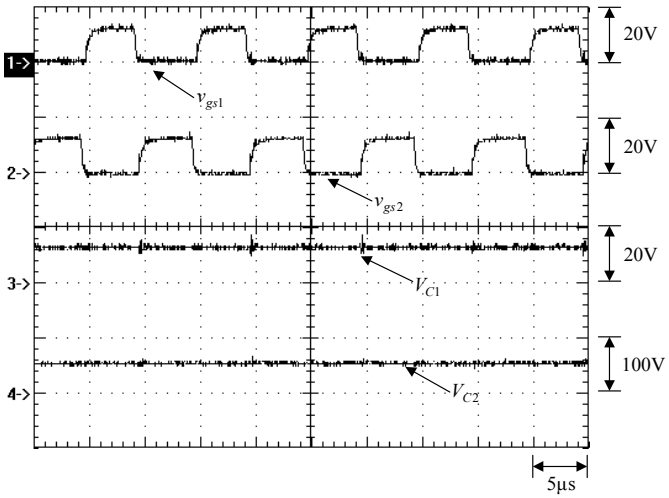

Fig. 17. Waveforms at light load: (1) v_{gs1}; (2) v_{gs2}; (3) V_{C1}; (4) V_{C2}.

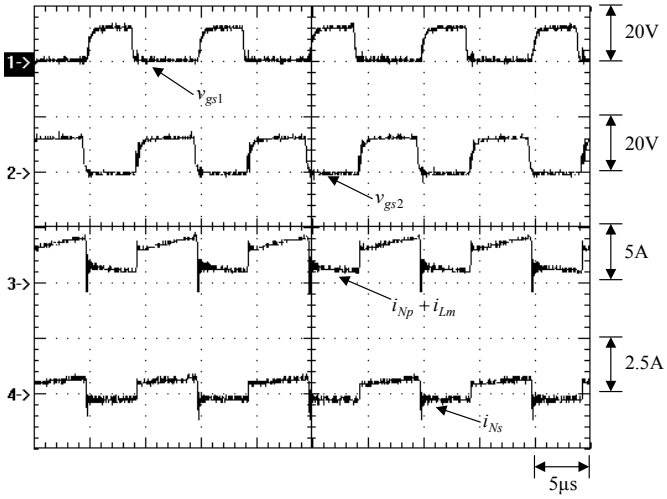

Fig. 18. Waveforms at half load: (1) v_{gs1}; (2) v_{gs2}; (3) i_{Np}+i_{Lm}; (4) i_{Ns}.

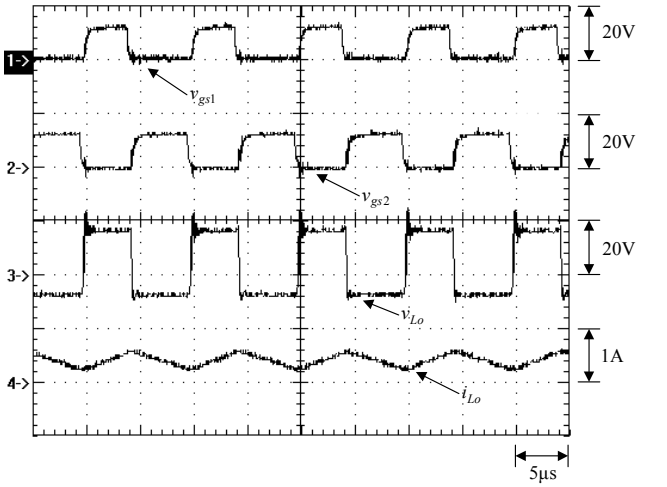

Fig. 19. Waveforms at half load: (1) v_{gs1}; (2) v_{gs2}; (3) v_{Lo}; (4) i_{Lo}.

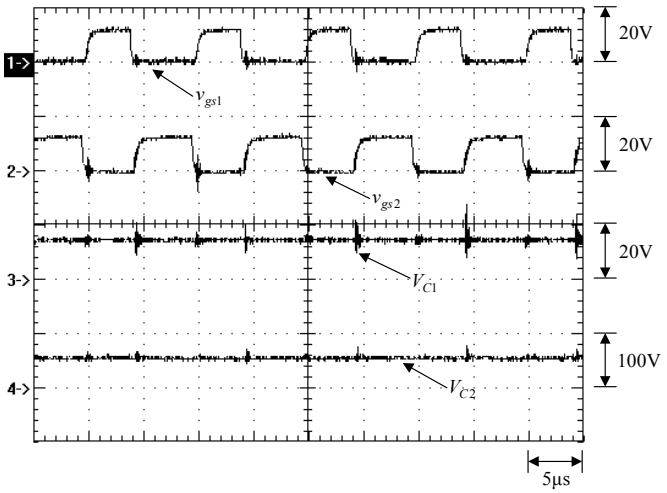

Fig. 20. Waveforms at half load: (1) v_{gs1}; (2) v_{gs2}; (3) V_{C1}; (4) V_{C2}.

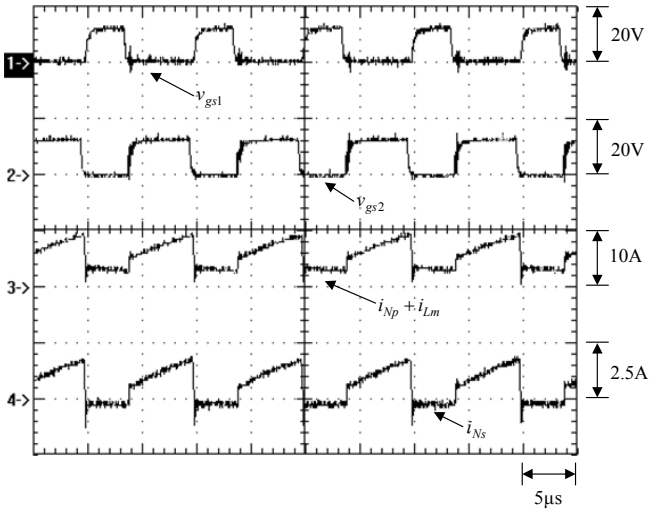

Fig. 21. Waveforms at rated load: (1) v_{gs1}; (2) v_{gs2}; (3) i_{Np}+i_{Lm}; (4) i_{Ns}.

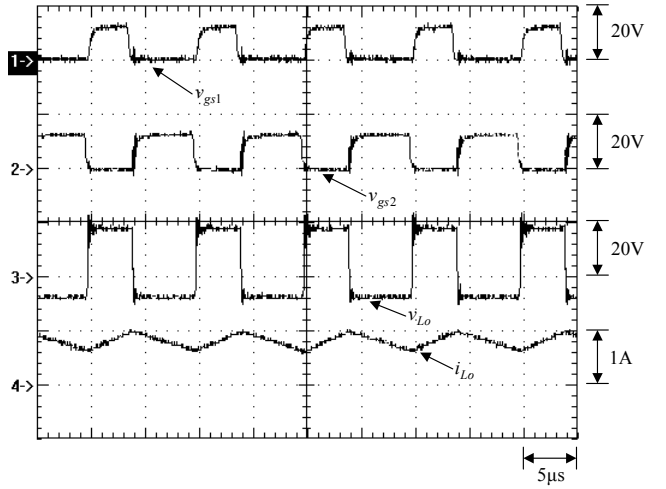

Fig. 22. Waveforms at rated load: (1) v_{gs1}; (2) v_{gs2}; (3) v_{Lo}; (4) i_{Lo}.

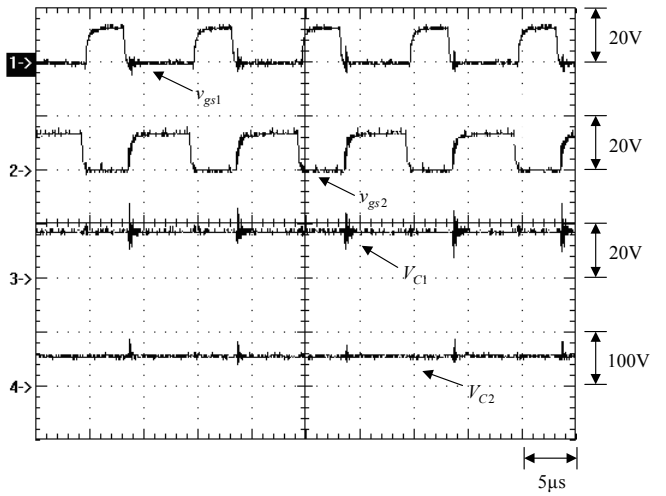

Fig. 23. Waveforms at rated load: (1) v_{gs1}; (2) v_{gs2}; (3) V_{C1}; (4) V_{C2}.

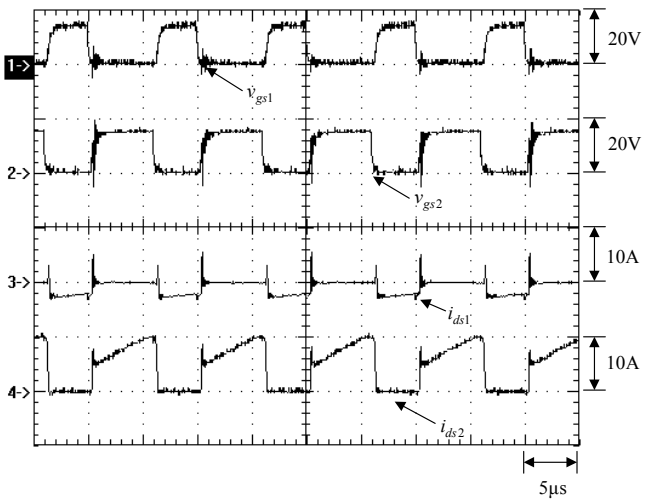

Fig. 24. Waveforms at rated load: (1) v_{gs1}; (2) $v_{gs2;}$ (3) i_{ds1}; (4) $i_{ds2.}$

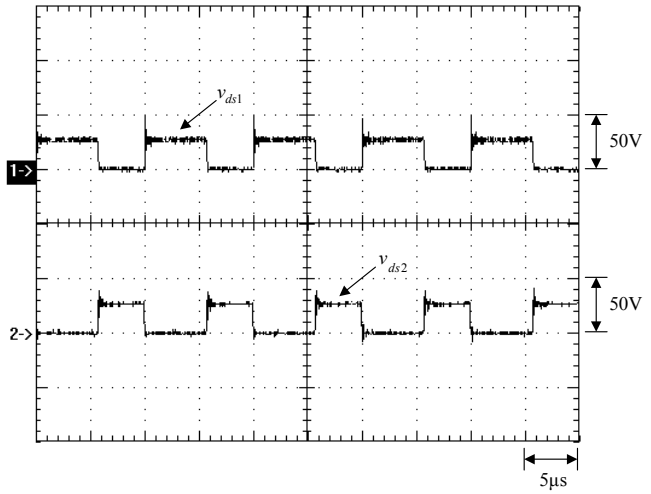

Fig. 25. Waveforms at rated load: (1) v_{ds1}; (2) $v_{ds2.}$

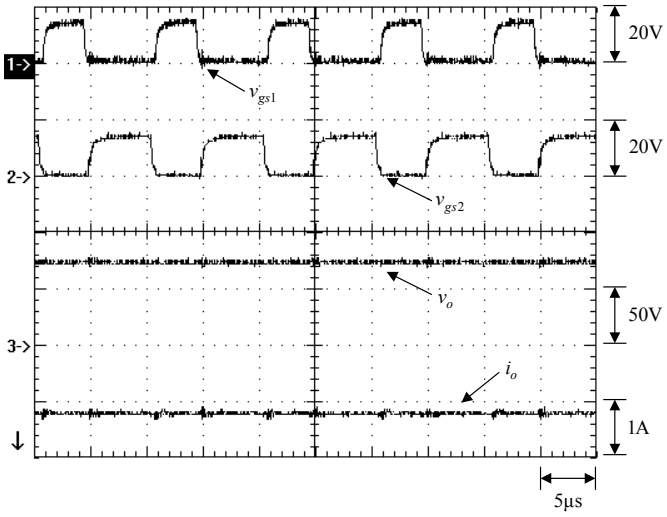

Fig. 26. Waveforms in the steady state at rated load: (1) v_{gs1}; (2) $v_{gs2;}$ (3) v_o; (4) $i_{o.}$

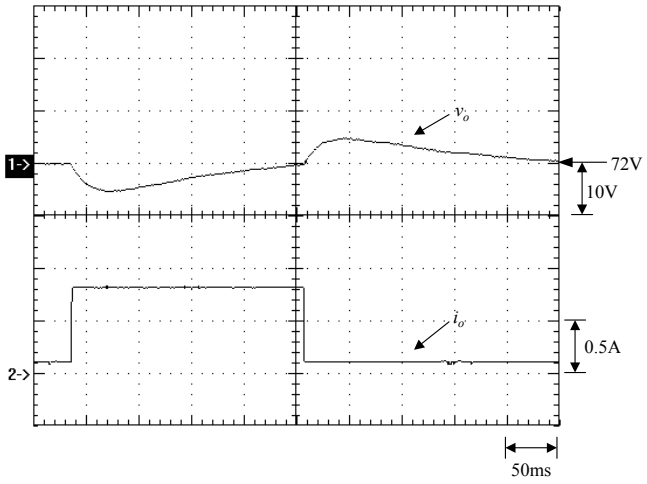

Fig. 27. Waveforms of load transient responses from light/rated load to rated/light load: (1) v_o; (2) $i_{o.}$

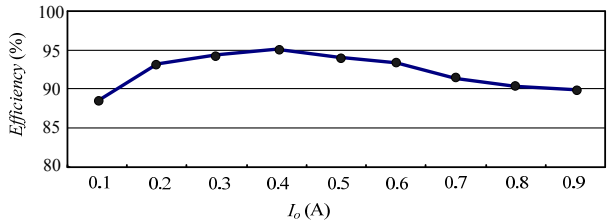

Fig. 28. Efficiency versus load current.

VI. CONCLUSION

A novel high step-up converter is presented herein. By combining the coupled inductor with the turns ratio, and the switched capacitor, the corresponding voltage gain is higher than that of the existing step-up converter combining KY and buck-boost converters. Furthermore, the proposed converter has no floating output, and has one output inductor so the output current is non-pulsating. Moreover, the structure of the proposed converter is quite simple and very suitable for industrial applications.

APPENDIX

Table III makes a comparison between the converters shown in the References, in terms of voltage gain, component number, switch voltage stress, output inductor and floating output.

Table III Comparison between the converters shown in the References, in terms of voltage gain, component number, switch voltage stress, output inductor and floating output

Ref.	Voltage gain	Component number	Switch voltage stress	Output inductor	Floating output
[3]	$\frac{1}{(1-D)^2}$	8	$V_{ds1}=\frac{V_i}{1-D}$, $V_{ds2}=V_{ds3}=\frac{V_i}{(1-D)^2}$	No	No
[4]	$\frac{1+n}{1-D}$	10	$V_{ds1}=nV_i$, $V_{ds2}=\frac{nD}{1-D}V_i$	No	No
[5]	$\frac{2+n}{1-D}$	10	$V_{ds1}=\frac{V_i}{1-D}$	No	No
[6]	$\frac{1+n}{1-D}$	15	$V_{ds1}=\frac{V_i}{1-D}$	No	No
[7]	$\frac{2}{1-D}+nD$	13	$V_{s1}=V_{s2}=\frac{V_o}{2}-\frac{nDV_i}{2}$	No	No
[8]	$\frac{1+D+nD}{1-D}$	9	$V_{ds1}=\frac{V_i}{1-D}$	No	Yes
[9]	$(\frac{2-D}{1-D})^n$ n: stage number	12, n=2 18, n=3	$[(\frac{2-D}{1-D})^n-(\frac{2-D}{1-D})^{n-1}]V_i$	No	No
[10]	$\frac{2(1+nD)}{1-D}$	10	$V_{ds1}=\frac{(1+nD)}{1-D}V_i$	No	Yes
[11]	$\frac{2+nD}{1-D}$	14	$V_{ds1}=\frac{V_o}{2}-\frac{nDV_i}{2(1-D)}$	No	No
[12]	$1+D$	6	$V_{ds1}=2V_i$, $V_{ds2}=V_i$	Yes	No
[13]	$\frac{2-D}{1-D}$	8	$V_{ds1}=V_{ds2}=\frac{V_i}{1-D}$	Yes	No
[14]	$\frac{2-D}{1-D}$	8	$V_{ds1}=V_{ds2}=\frac{V_i}{1-D}$	Yes	No
[15]	$\frac{2}{1-D}+n$	8	$V_{ds1}=V_{ds2}=\frac{V_i}{1-D}$	No	No
[16]	Type 1: $\frac{3-D}{1-D}$ Type 2: $\frac{2}{1-D}$ Type 3: $\frac{3-2D}{1-D}$	10	Type 1: $V_{ds1}=V_{ds2}=V_i$ $V_{ds3}=V_o-2V_i$ Type 2: $V_{ds1}=V_{ds2}=V_i$ $V_{ds3}=V_o-V_i$ Type 3: $V_{ds1}=V_{ds2}=V_i$ $V_{ds3}=V_o-V_i$	No	No
[17]	$\frac{2nD}{1-D}+1$	11	$V_{ds1}=V_i$, $V_{ds2}=V_i$ $V_{ds3}=(\frac{3D-1}{1-D})V_i$	No	No
[18]	Type 1: 2D Type 2: 2D	8	Type 1: $V_{ds1}=V_i$, $V_{ds2}=V_i$ $V_{ds3}=V_i$, $V_{ds4}=V_i$ Type 2: $V_{ds1}=V_i$, $V_{ds2}=V_i$ $V_{ds3}=V_i$, $V_{ds4}=V_i$	Yes	No

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