Three-Phase Soft-Switching Inverter With Minimum Components

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***Abstract*—In this paper, a novel three-phase soft-switching inverter is presented. The inverter-switch turn on and turn off are performed under zero-voltage switching condition. This inverter has only one auxiliary switch, which is also soft switched. Having one auxiliary switch simplifies the control circuit considerably. The proposed inverter is analyzed, and its operating modes are explained in details. The design considerations of the proposed inverter are presented. The experimental results of the prototype inverter confirm the theoretical analysis.**

***Index Terms*—Quasi-resonant dc link (QRDCL), soft-switching inverter, zero-voltage switching (ZVS).**

I. Introduction

INVERTERS have many applications in power-electronic devices, such as motor drives, active-power filters, and uninterruptible power supplies. In order to reduce the size of output filter and eliminate audio noise, switching frequency must be increased. In hard-switching inverters, higher switching frequency leads to increased switching losses, which consequently increase the size of snubber circuits and heatsinks. In addition, electromagnetic interference increases, and efficiency is decreased [1]. To overcome these problems, applying soft-switching techniques is essential [2]–[9].

Quasi-resonant dc-link (QRDCL) inverters are one type of soft-switching inverters that can be controlled by pulsewidth modulation (PWM) method [10]–[22]. In these inverters, the input power supply is separated from the inverter dc link by a switch, called dc-link switch. Also, a resonant capacitor is placed in parallel with the inverter dc link. When a change in the state of inverter switches is necessary, the dc-link switch is turned off, and the resonant capacitor discharges by an auxiliary circuit, and thus, the state of inverter switches can be changed under zero-voltage switching (ZVS) condition. The auxiliary circuit usually requires two switches or more in order to charge and discharge the dc-link capacitor. Since all QRDCL inverters require a switch in their main power path, they are suitable for medium- and low-power applications.

One of the main QRDCL inverter research goals is to achieve soft-switching condition with minimum number of auxiliary-circuit elements. The auxiliary circuits in [10] and [11] have three auxiliary switches, and the auxiliary circuits in [12]–[18] have two switches. Reducing the auxiliary-circuit switches simplifies the control circuit and decreases the inverter cost. Therefore, it is essential to offer QRDCL inverters with one switch in the auxiliary circuit [19], [20]. In [19], the number of switches in the auxiliary circuit is reduced at the cost of employing extra circuit elements, including three diodes, a pair of coupled inductors, and a resonant capacitor. The auxiliary circuit presented in [20] has reduced the number of extra elements at the expense of adding a capacitive voltage divider at the inverter input. In addition, the control over the zero-voltage interval of this inverter dc link is lost. The control of the dc-link zero-voltage interval is used in some switching methods such as space vector modulation (SVM).

In this paper, a QRDCL inverter without any switch in its auxiliary circuit is presented. All semiconductor components are soft switched. The dc-link switch is turned on under zero-current switching (ZCS) condition and turned off under almost ZVS condition. Also, the auxiliary diode in this circuit turns on under ZVS condition and turns off under ZCS condition. The proposed inverter has the least number of extra elements in comparison with previous QRDCL inverters. The proposed inverter was originally introduced in [21], but in power factors below 0.87, soft-switching conditions are lost. In this paper, the weaknesses are eliminated by modifying the operating modes. Furthermore, the practical results, along with more comprehensive analysis, are included.

The proposed inverter is introduced, and its modified operating modes are discussed in Section II. Design considerations of the proposed inverter are provided in Section III, and the experimental results of a prototype inverter are presented in Section IV. The presented experimental results confirm the theoretical analysis.

II. Proposed Inverter Description and Operation

A. Operating Modes

The circuit configuration of the proposed QRDCL inverter is shown in Fig. 1. The main inverter is composed of S_1 to S_6. The dc-link switch is S_a, and the dc-link resonant capacitor is C_r. The auxiliary circuit consists of diode D and coupled inductors L_{r1} and L_{r2}. Because the inductors L_{r1} and L_{r2} are much smaller than the load inductance, the inverter with a three-phase load can be replaced by the current source I_o, as shown in Fig. 2. I_o abruptly alters when the state of the inverter switches changes. In order to simplify the description of the inverter operating intervals, all circuit elements are assumed ideal.

The proposed inverter has seven distinct operating modes in a switching cycle. The main theoretical waveforms of the inverter

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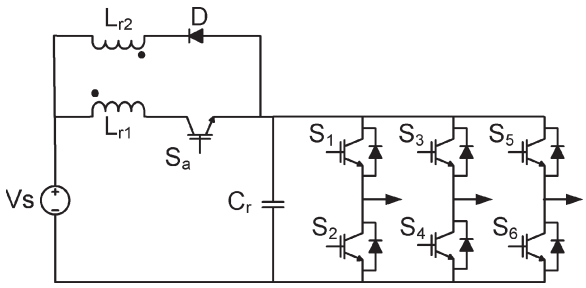

Fig. 1. Power circuit configuration of the proposed QRDCL inverter.

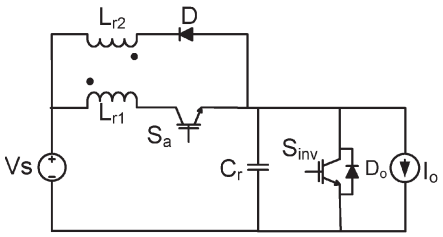

Fig. 2. Equivalent circuit of the proposed inverter.

in the distinguished modes are shown in Fig. 3. The equivalent circuit of each operating mode is shown in Fig. 4. Before the first operating interval, it is supposed that $\mathrm{S_{inv}}$ is on, and the output current I_o freewheels through $\mathrm{D_o}$.

Mode 1 $(t_0 \le t \le t_1)$*:* At t_0, $\mathrm{S_a}$ is turned on. Due to the existence of L_{r1}, the turning on of $\mathrm{S_a}$ is under ZCS condition, and the L_{r1} current increases linearly. The inductor current is

$$I_{Lr1}(t) = \frac{V_s}{L_{r1}}(t - t_0). \tag{1}$$

The inductor current increases until it reaches I_i. I_i is defined as the minimum required current of L_{r1} that guarantees discharging C_r in Mode 4. The design procedure of I_i is illustrated in Section III. The duration of this mode is

$$\Delta t_1 = t_1 - t_0 = \frac{L_{r1} I_i}{V_s}. \tag{2}$$

Mode 2 $(t_1 \le t \le t_2)$*:* At t_1, the state of the inverter main switches is changed. Due to the zero voltage of C_r, these changes are under ZVS conditions. In other words, in the equivalent circuit, $\mathrm{S_{inv}}$ is turned off. Thus, C_r resonates with L_{r1}, and its voltage increases. The C_r voltage and L_{r1} current are

$$V_{Cr}(t) = Z_r(I_i - I_o)\sin(\omega_r(t - t_1)) + V_s(1 - \cos(\omega_r(t - t_1))) \tag{3}$$

$$I_{Lr1}(t) = (I_i - I_o)\cos(\omega_r(t - t_1)) + \frac{V_s}{Z_r}\sin(\omega_r(t - t_1)) + I_o \tag{4}$$

where

$$\omega_r = \frac{1}{\sqrt{L_{r1}C_r}} \tag{5}$$

$$Z_r = \sqrt{\frac{L_{r1}}{C_r}}. \tag{6}$$

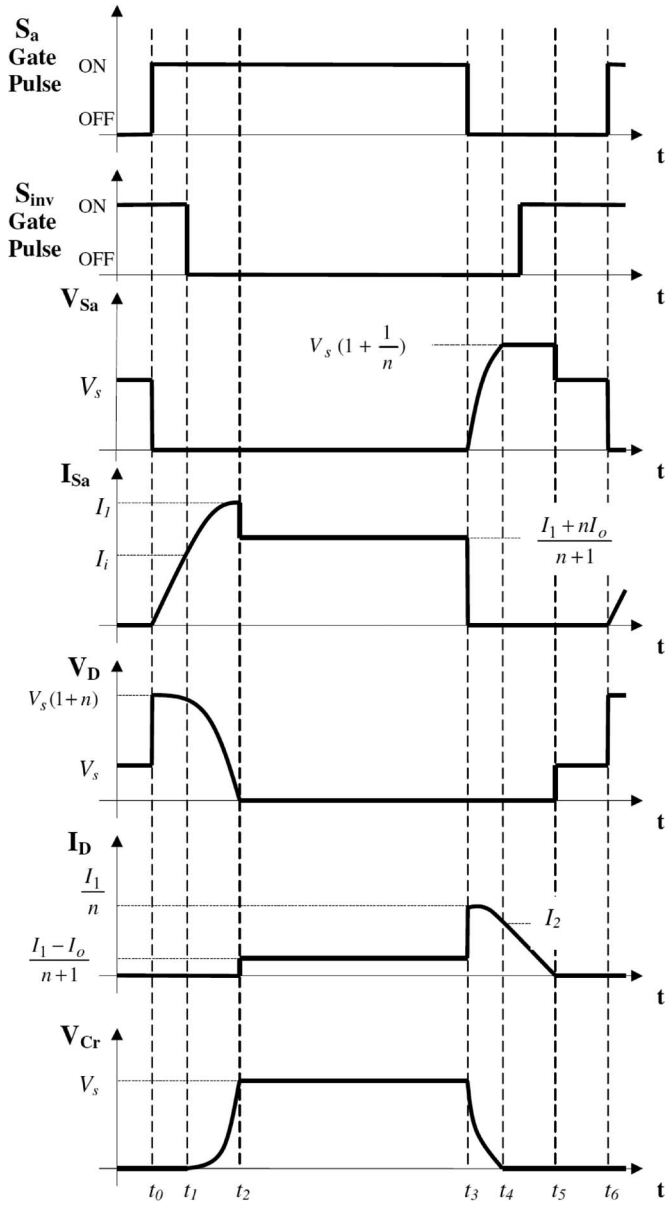

Fig. 3. Main theoretical waveforms of the proposed inverter.

This mode continues until V_{Cr} reaches V_s. Therefore, the duration of this mode is

$$\Delta t_2 = t_2 - t_1 = \frac{1}{\omega_r}\tan^{-1}\left(\frac{V_s}{Z_r(I_i - I_o)}\right). \tag{7}$$

Mode 3 $(t_2 \le t \le t_3)$*:* At t_2, the C_r voltage reaches V_s, and diode D turns on at ZVS condition. Thus, a fraction of the flux linkage of L_{r1} moves to L_{r2}. At the beginning of this mode, the L_{r1} current is

$$I_{Lr1}(t_2) = I_1 = \sqrt{\left(\frac{V_s}{Z_r}\right)^2 + (I_i - I_o)^2} + I_o. \tag{8}$$

The aforementioned relation is obtained by substituting t in (4) with Δt_2 from (7).

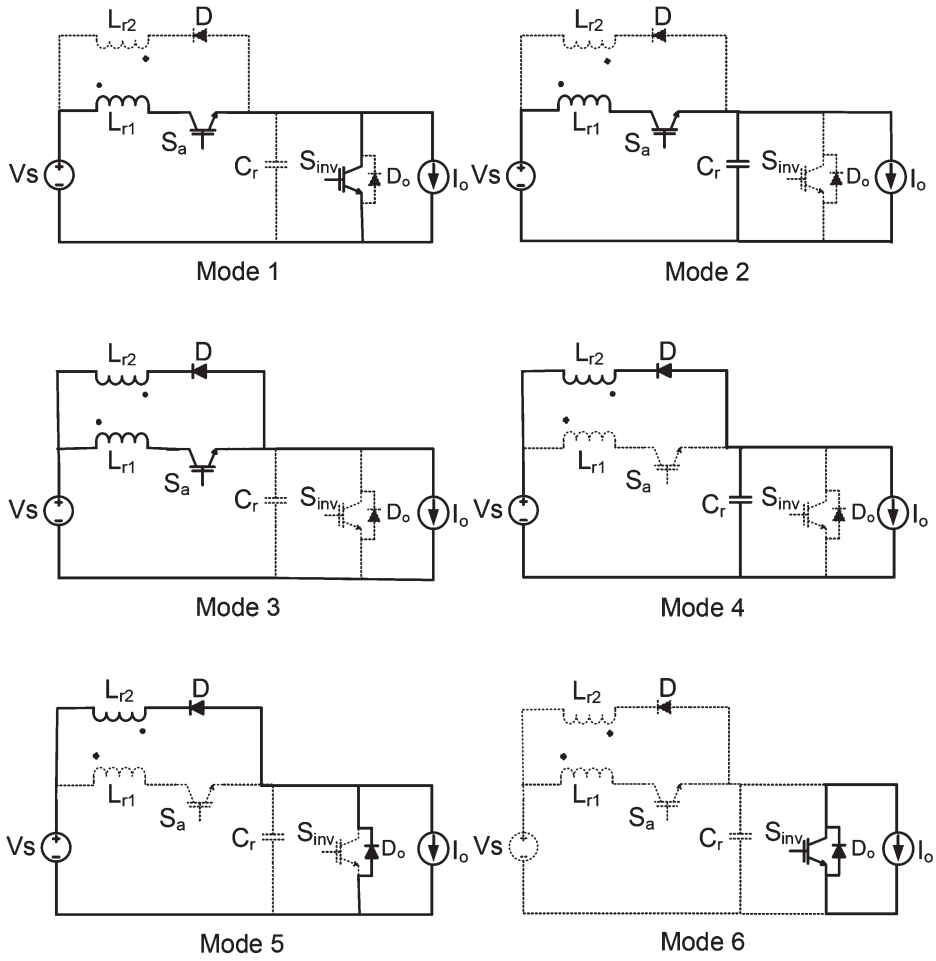

Fig. 4. Equivalent circuit of each operating mode.

The ampere-turns of the coupled inductors must be constant, thus

$$N_1 I_1 = N_1 I_{Lr1} + N_2 I_{Lr2} \tag{9}$$

where I_{Lr1} and I_{Lr2} are the currents of L_{r1} and L_{r2}, and N_1 and N_2 are inductor-winding turns of L_{r1} and L_{r2}, respectively. The Kirchhoff's current law equation at the output node is

$$I_{Lr1} = I_{Lr2} + I_o. \tag{10}$$

By substituting (10) into (9), the following are obtained:

$$I_{Lr1} = \frac{I_1 + nI_o}{n+1} \tag{11}$$

$$I_{Lr2} = \frac{I_1 - I_o}{n+1} \tag{12}$$

where $n = N_2/N_1$. In this mode, energy flows from the input power supply to the load. This mode continues, while the states of the inverter main switches need to change.

Mode 4 $(t_3 \le t \le t_4)$*:* If the inverter main switches require changing, the dc-link voltage must be reduced to zero. Thus, in this mode, switch $\mathrm{S_a}$ is turned off, and the L_{r1} energy is transferred to L_{r2}. C_r resonates with L_{r2}, and its voltage decreases. At t_3, the C_r voltage is V_s; therefore, $\mathrm{S_a}$ is turned off under ZVS condition. In practice, the leakage inductance of the coupled inductors degrades the soft switching to almost ZVS condition at turn off. The C_r voltage and L_{r1} current in this mode are

$$V_{Cr}(t) = V_s - Z_r I_1 \sin\left(\frac{\omega_r}{n}(t - t_3)\right) \tag{13}$$

$$I_{Lr2}(t) = \frac{I_1}{n} \cos\left(\frac{\omega_r}{n}(t - t_3)\right). \tag{14}$$

This mode continues until the C_r voltage reaches zero. The duration of this mode is

$$\Delta t_4 = t_4 - t_3 = \frac{n}{\omega_r} \sin^{-1}\left(\frac{V_s}{Z_r I_1}\right). \tag{15}$$

Mode 5 $(t_4 \le t \le t_5)$*:* In this mode, $\mathrm{D_o}$ turns on under ZVS condition, and the L_{r2} current flows to the input source. Its current decreases linearly from I_2 to zero. The L_{r2} current in this mode is

$$I_{Lr2}(t) = I_2 - \frac{V_s}{L_{r2}}(t - t_4) \tag{16}$$

where

$$I_2 = I_{Lr2}(t_4) = \frac{1}{n}\sqrt{I_1^2 - \left(\frac{V_s}{Z_r}\right)^2}. \quad (17)$$

In this mode, S_{inv} can be turned on under ZCS condition, and the S_a voltage reaches its maximum value as

$$V_{Sa,\max} = V_s\left(1 + \frac{1}{n}\right). \quad (18)$$

The duration of this mode is

$$\Delta t_5 = t_5 - t_4 = \frac{L_{r2} I_2}{V_s}. \quad (19)$$

Mode 6 ($t_5 \le t \le t_6$)*:* At t_5, the L_{r2} current reaches zero, and D_1 and D_o turn off at ZCS condition. Notice that in some switching methods, such as SVM, this mode can be used as zero vector.

B. Comparison

In this section the proposed inverter and the inverter of [21] are compared. These two inverter configurations are similar. They use minimum components to achieve soft-switching conditions for the inverter main switches. The difference is only in their operating modes. The inverter of [21] does not short circuit the dc link by turning on two switches of one inverter leg. However, the proposed inverter in this paper performs this task in order to overcharge the coupled inductors. Thus, enough energy for discharging the dc-link capacitor at all conditions is stored in the coupled inductors.

In motor-drive applications, the inverter should be able to return some of the energy from the load to the supply at regeneration mode. In addition, at power factors lower than 0.87, I_o (as shown in Fig. 2) is sometimes negative in a period of output waveform. In these cases, the inverter of [21] loses soft-switching condition.

In this paper, the aforementioned drawback is overcome, and soft switching is achieved at any condition. In Mode 4, I_1 must be large enough to discharge C_r. I_1 is defined in (8). According to this equation, even when I_o is negative, I_i can be increased to any desired value by increasing I_1. Increasing I_i is achieved by keeping the dc-link switch and two switches of one inverter leg at ON state. This change in operating modes should be considered in the control circuit. The control circuit is explained in the next section.

III. Design Considerations

A. Inverter Elements

Designing the proposed inverter involves the selection of L_{r1}, C_r, n, I_i, switch S_a, and diode D. L_{r1} provides ZCS condition for auxiliary switch at the turn-on instant. This inductor can be designed like a regular turn-on snubber [22]. C_r provides ZVS condition at switch turn-off instant for the main switches and the auxiliary switch. Therefore, its value can be selected like a regular turn-off snubber [22].

It can be observed from (12) and (18) that as n increases, the auxiliary-switch voltage stress (in the fourth mode) and the freewheeling current (in the third mode) decrease. However, this results in higher voltage stress of diode D. In practice, n is selected to be between two and three. Thus, the voltage stress of D is

$$V_{D,\max} = V_s(1+n). \quad (20)$$

For high input voltages, a high-voltage diode is required. This is not a limitation since high-voltage fast-recovery diodes, such as BYV26G, are available.

I_i must be large enough to guarantee discharging C_r in Mode 4. According to (13), to guarantee discharging C_r to zero, the following relation must be held:

$$Z_r I_1 \ge V_s. \quad (21)$$

By substituting I_1 from (8) to (21), the following relation is obtained:

$$I_i \ge I_o + \sqrt{I_o^2 - 2I_o\frac{V_s}{Z_r}}. \quad (22)$$

It is required to design for the worst condition and convert relation (22) to an equation. The right side of (22) is maximum when I_o is maximized. Thus, the following is obtained:

$$I_i = I_{om} + \sqrt{I_{om}^2 - 2I_{om}\frac{V_s}{Z_r}} \quad (23)$$

where I_{om} is the maximum of I_o.

B. Switch Gate Pulses

The control of the main inverter switches is the same as with conventional PWM inverters. PWM pulses can be extracted by comparing a sawtooth waveform with three 120°-shifted sine waves. When a change in the state of one inverter-leg switches is required, S_a must be turned off prior to applying gate pulses to the inverter-leg switches. Thus, the state of the main inverter switches must be changed after a delay. This delay, as shown in Fig. 5 is named as PWM delay and is the required time for C_r to be discharged. This time can be obtained from (15).

The required change in the state of each PWM generator can be detected with one monostable. The output pulses of these monostables go through a logical AND. The resulting pulse is used to turn off S_a and must be greater than the PWM delay to guarantee changing the inverter main switches at ZVS condition.

When S_a is turned on again, S_{inv} must turn on simultaneously to increase the L_{r1} current to I_i, as obtained from (23). Therefore, the S_{inv} on time can be calculated from (2). The S_{inv} gate pulse can be created by another monostable. Turning S_{inv} on means that the inverter dc link is short circuited. This condition can be achieved by turning on only the switches of one inverter leg, such as S5 and S6.

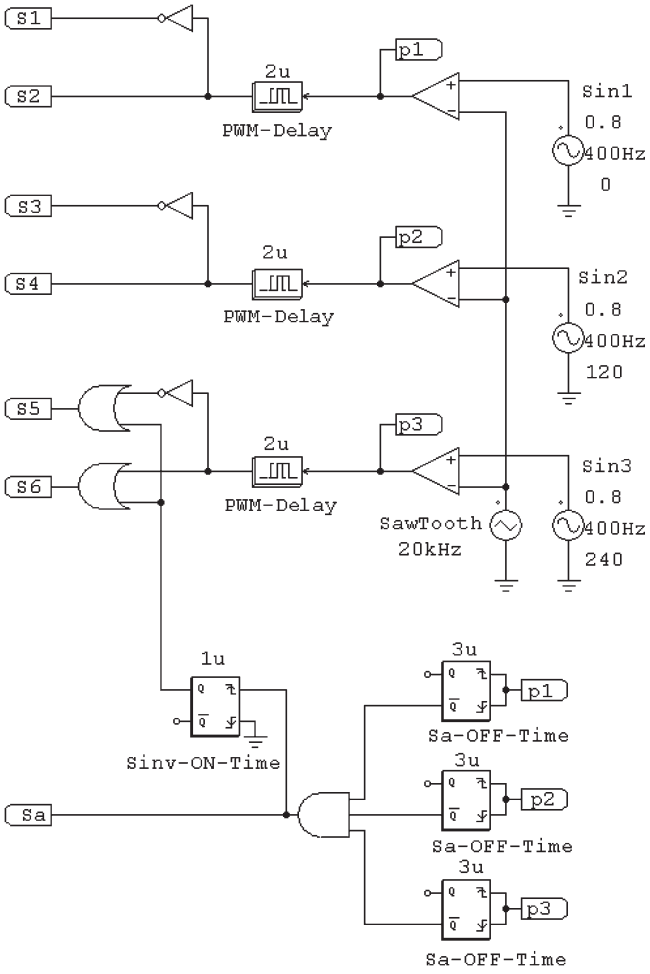

Fig. 5. Gate-pulse generation circuit.

IV. Experimental Results

A prototype of the proposed soft-switching inverter is implemented at 20-kHz switching frequency. The input voltage (V_s) is 100 V, and the output load power is 250 W with 0.8 power factor. The output frequency is 400 Hz. According to the design procedure, the auxiliary-circuit parameters are calculated as $C_r = 10$ nF, $L_{r1} = 17$ μH, and $n = 2$. L_{r1} and L_{r2} are very small and are realized by winding five and ten turns, respectively, on EI2820 ferrite core using a small air gap. All switches are IRF640, and the diode is MUR460.

The experimental results are shown in Figs. 5–8. The S_a voltage and current are shown in Fig. 6. As seen in this figure, S_a is turned on at ZCS condition and is turned off at ZVS condition. Also, the diode D turn on and turn off are at ZVS and ZCS conditions, respectively, as shown in Fig. 7.

In Mode 6, the parasitic oscillations on the voltage waveforms across S_a and diode D are due to resonance between the switch drain–source capacitor and the coupled inductors. At the end of Mode 5, the drain–source capacitor voltage of S_a is $V_s(1 + (1/n))$. This voltage at the beginning of Mode 6 must be reduced abruptly to V_s. Therefore, the S_a drain–source capacitor resonates with L_{r1}. In this resonance, the voltage of L_{r2} (which is coupled with L_{r1}) is changed in a resonant

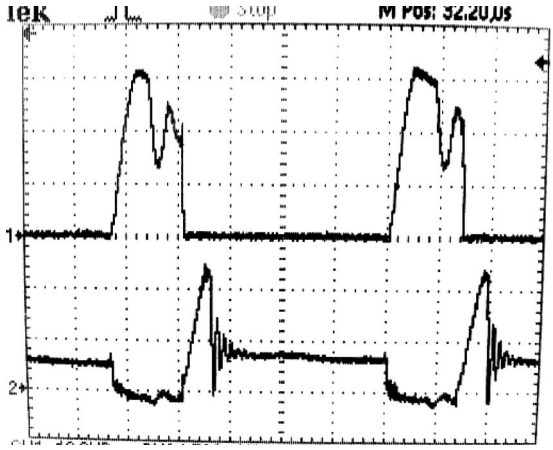

Fig. 6. Top: S_a voltage (50 V/div) and bottom: S_a current (2.5 A/div). (Time: 2.5 μs/div).

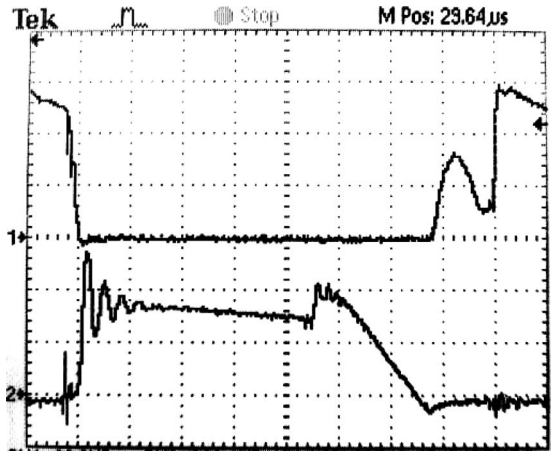

Fig. 7. Top: Diode D voltage (100 V/div) and bottom: diode D current (1 A/div). (Time: 1 μs/div).

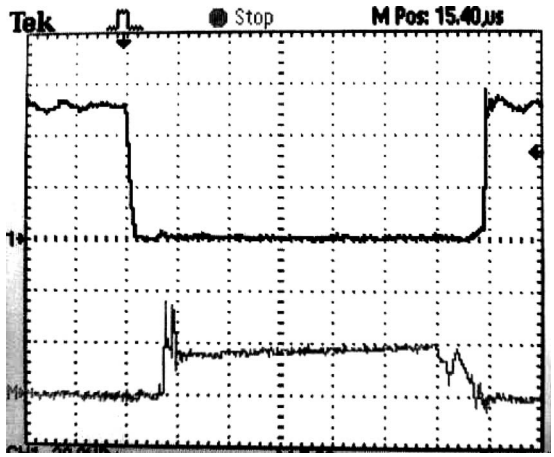

Fig. 8. Top: S_1 voltage (40 V/div) and bottom: S_1 current (1 A/div). (Time: 5 μs/div).

fashion, and, similarly, the voltage of diode D increases from zero to V_s.

The small parasitic oscillations on S_a and diode D currents are due to the resonance between C_r and the small leakage inductance of the coupled inductors. At the beginning of Mode 3, when the C_r voltage reaches V_s, diode D is forward

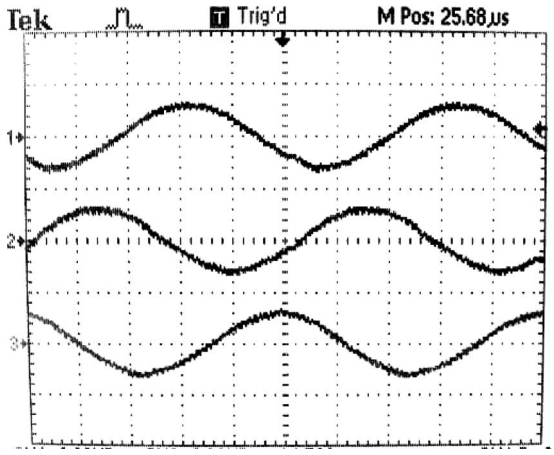

Fig. 9. Output three-phase current (10 A/div). (Time: 500 μs/div).

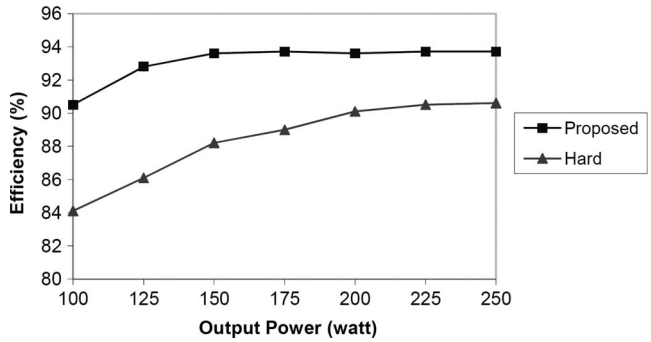

Fig. 10. Efficiency comparison of the proposed converter versus hard-switching counterpart.

biased, and its current must increase abruptly if there were no inductance in its path. However, due to the existence of small leakage inductance of the coupled inductors, this current cannot change abruptly and increases in a resonant fashion.

Fig. 8 shows one of the inverter main switches voltage and current which are turned on and turned off under ZVS condition. The three-phase output currents are shown in Fig. 9. The converter efficiency versus output power is shown in Fig. 10. As can be observed, the efficiency of soft-switching converter has improved by 3%, in comparison with the hard-switching counterpart, at full load.

V. Conclusion

In this paper, a new soft-switching three-phase inverter with one dc-link switch has been presented. All switches and diodes in this inverter are soft switched, although it has a lower number of extra elements than the previous soft-switching inverters. In addition, all semiconductor elements are soft switched. A prototype of this inverter has been implemented. The presented experimental results confirm the theoretical analysis.

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