Low-Cost Semi-Z-source Inverter for Single-Phase Photovoltaic Systems

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***Abstract*—This paper presents several nonisolated semi-Z-source inverters for a single-phase photovoltaic (PV) system with low cost and doubly grounded features. These semi-Z-source inverters employ the Z-source/quasi-Z-source network and only two active switches to achieve the same output voltage as the traditional voltage-fed full-bridge inverter does. The two active switches of the semi-Z-source inverter are controlled complementarily. Different from the traditional single-phase Z-source/quasi-Z-source inverter, shoot-through zero state is not applicable to the semi-Z-source inverter. The input dc source and the output ac voltage of the semi-Z-source inverter share the same ground, thus leading to less leakage ground current advantages over other nondoubly grounded inverters, such as voltage-fed full-bridge inverter. This is a preferred feature for nonisolated grid-connected inverters, especially in PV application. A revised nonlinear sinusoid pulse width modulation method for a semi-Z-source inverter is also proposed. By using this method, desired duty cycle can be generated to output the sinusoidal voltage. Other dc–dc converters with similar voltage gain curve, which can also be used as a single-phase inverter, are also discussed and summarized. A single-phase semi-Z-source inverter prototype is built; experimental results are provided to verify and demonstrate the special features of the proposed circuit.**

***Index Terms*—Inverter, low cost, photovoltaic (PV), quasi-Z-source, semi-Z-source.**

I. Introduction

In RECENT years, due to energy crisis, renewable energy distributed power generators (DGs), such as wind turbine, photovoltaic (PV) cell, fuel cell, and thermoelectric generation (TEG) modules, are becoming more and more popular in industrial and residential applications [1]. Many renewable energy DGs such as PV cell, fuel cell, and TEG module can only output dc voltage, so an inverter interface has to be utilized for grid-connected applications [2], [3]. Many inverter topologies have been proposed and reviewed recently [4]–[12].

Based on galvanic isolation, these inverters can be divided into two categories: isolated inverters and nonisolated inverters. Isolated inverters usually utilize a line frequency or high-frequency transformer for electrical isolation. Due to size, weight, and cost considerations, high-frequency transformers are inclined to be used for future applications [7]. For the inverter topologies with a high-frequency transformer, there are several popular approaches. The first approach is a single-stage isolated buck–boost inverter or flyback inverter [13]–[22]. This approach usually utilizes less switching devices, and is able to eliminate electrolytic capacitors by using high-voltage low-capacitance film or ceramic capacitor for energy storage [7], [14]–[17]. The second approach is a two-stage approach, with an isolated dc–dc converter in the first stage and a full-bridge inverter in the second stage [23]–[31]. A high-efficiency high-voltage gain dc–dc converter with soft switching can be designed for the first stage [10], [30]. The second full-bridge inverter stage can utilize high-frequency switches with pulse width modulation (PWM) strategy or line frequency switches just for voltage inversion purposes based on different topologies. The third approach is also a two-stage approach with a high-frequency dc–ac inverter, a high-frequency transformer, and an ac–ac converter [10], [32]. Transformer-isolated topologies usually have higher voltage gain and safety advantages, but they require more switches with relatively high cost, high complexity, and low system efficiency.

In some countries, galvanic isolation is not a requirement in the low-voltage grid or power levels below 20 kW [33]. This leads to the development of low-cost transformer-less inverter topologies. The transformer-less inverter topologies can be classified into two categories: two-stage inverter topologies and single-stage inverter topologies [34]–[49]. The two-stage transformer-less inverter topologies are similar in operation to the second approach of the aforementioned transformer isolated topologies. Different from that approach, a nonisolated dc–dc converter is used in the first stage instead [34]–[36], [38], [42], [45]–[47]. In most cases, a full-bridge inverter with line frequency switched devices is used in the second stage to reduce the cost and the switching loss. To further simplify the system complexity and to reduce the cost, single-stage inverter topologies are investigated. The single-stage inverter approach usually consists of two relatively independent dc–dc converters with possible shared passive components and each converter produces a half-cycle sinusoid waveform 180° out of phase [10], [37], [39]–[41], [43], [44], [48]. However, for the transformer-less inverter topologies, if the input dc-source and the grid do not share the same ground, the input dc source, especially for PV cell, may have large leakage current, which will cause safety and electromagnetic interference problems [6], [33], [50].

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In order to solve this problem, either extra switches have to be added to the existing topology which will inevitably increase the cost and system complexity or doubly grounded topologies have to be used [6], [33], [40], [50]–[55]. Therefore, for the considerations of safety, cost, and system simplicity, the doubly grounded nonisolated inverter topologies are preferred topologies for the renewable DG in grid-connected application.

To reduce the cost and to increase the system reliability, Z-source and quasi-Z-source inverter as a single-stage transformer-less inverter topology is proposed [56]–[58]. By utilizing the unique *LC* network, a shoot-through zero state can be added to replace the traditional zero state of the inverter and to achieve the output voltage boost function. Many different PWM strategies have been proposed to control the Z-source inverter or multilevel Z-source inverter based on different methods of placing the shoot-through zero state [59]–[67]. Traditionally, Z-source and quasi-Z-source inverters are applied to the three-phase PV or wind power grid-connected generation systems, or three-phase motor drive for hybrid electric vehicle (HEV) application [68]–[76]. Recently, many Z-source/modified Z-source single-phase inverters have been proposed for PV, motor drive, or UPS applications [77]–[86]. Most of these topologies do not have the aforementioned doubly grounded features except [85]. But [85] only provide the Z-source approach with one cycle control. The control differences of the proposed single-phase Z-source inverter with other traditional single-phase Z-source inverter are not discussed. The corresponding quasi-Z-source inverter derived topology is not discussed either.

This paper presents a family of single-stage nonisolated semi-Z-source inverters that can be used for the aforementioned renewable DG grid-connected application with low cost and doubly grounded features. The proposed circuit can achieve the same output voltage as the traditional voltage-fed full-bridge inverter does, with only two active switches. Compared with the traditional single-phase Z-source inverters, the proposed semi-Z-source inverters share the same form of Z-source network. But the Z-source network used in semi-Z-source inverter is in ac side, which is smaller in size than the traditional Z-source network used in dc side. The modulation strategy of the proposed circuit is also different. The traditional Z-source inverters use sinusoidal reference with extra shoot-through reference to output sinusoid voltage and achieve the voltage boost function. However, in order to output sinusoid voltage, the semi-Z-source inverter has to utilize its nonlinear voltage gain curve to generate a modified voltage reference. These differences are the reasons why the author uses the term semi-Z-source inverter to represent the proposed topologies and to distinguish it from the traditional single-phase Z-source inverter. The circuit operation and the modulation strategy of the proposed topology are analyzed in detail and verified by the experimental results.

II. Proposed Semi-Z-Source/Semi-Quasi-Z-Source Inverters and Topology Derivations

Figs. 1 and 2 show the Z-source and quasi-Z-source dc–dc converters with input and output sharing the same ground [87]. Fig. 1 shows the Z-source and quasi-Z-source dc–dc converter topologies with discontinuous voltage gain curve, as shown in Fig. 3(a). Fig. 2 shows the two topologies with continuous voltage gain curve, as shown in Fig. 3(b). The duty cycle of S_1 is defined as D. And the voltage gain equation in terms of D is also shown in Fig. 3. All of these four topologies can output positive and negative voltages when the duty cycle is changed from 0 to 1. But only the topologies shown in Fig. 2 can output the positive and negative voltages with continuous voltage gain curve. This means that these two topologies can be used as an inverter by providing proper modulation strategy with the duty cycle D changed from 0 to 2/3. And the output voltage range of the inverter is the same as that of the full-bridge inverter, which is $-V_{\rm in}$ to $+V_{\rm in}$. Fig. 4 shows the proposed single-phase semi-Z-source and semi-quasi-Z-source inverters based on the different impedance network. The semi-Z-source inverter, as shown in Fig. 4(a), is already discussed in [85]. This paper will concentrate on semi-quasi-Z-source inverter and the PWM control strategy. For the proposed semi-Z-source and quasi-Z-source inverter, only two bidirectional current conducting and unidirectional voltage blocking switching devices, such as insulated gate bipolar transistor (IGBT) and MOSFET, are needed for the operation. Because the voltage gain of the full-bridge inverter is a straight line, the sinusoidal PWM (SPWM)

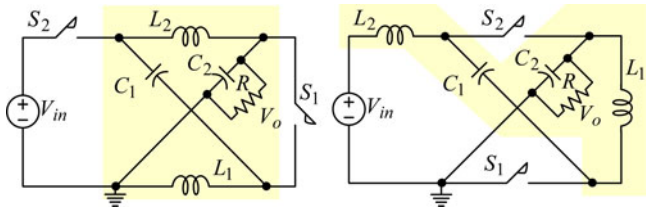

Fig. 1. Z-source and quasi-Z-source dc–dc converters with discontinuous voltage gain, as shown in Fig. 3(a).

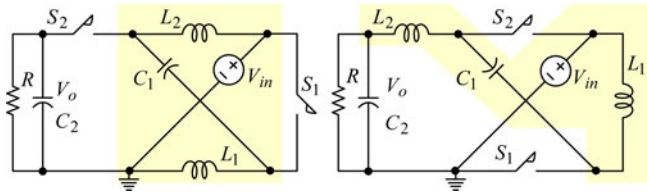

Fig. 2. Z-source and quasi-Z-source dc–dc converters with continuous voltage gain, as shown in Fig. 3(b).

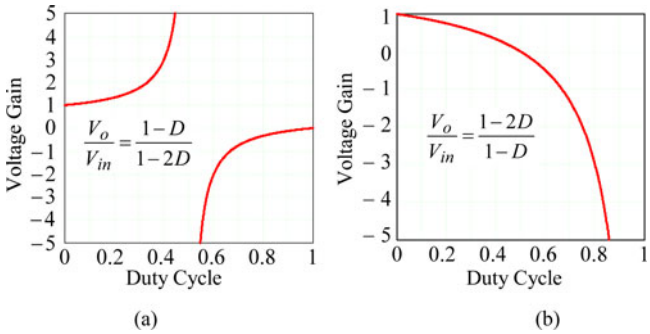

Fig. 3. Voltage gain curve of Z-source and quasi-Z-source dc–dc converters as shown in Figs. 1 and 2.

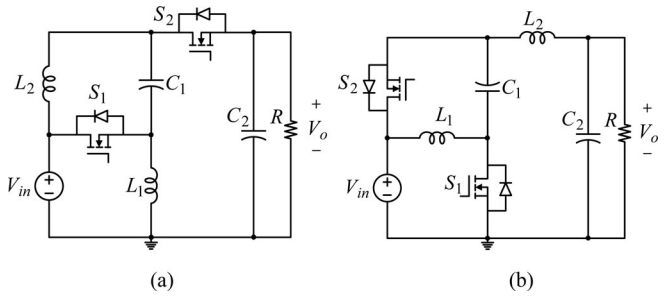

Fig. 4 Proposed single-phase semi-Z-source inverters. (a) Semi-Z-source inverter. (b) Semi-quasi-Z-source inverter.

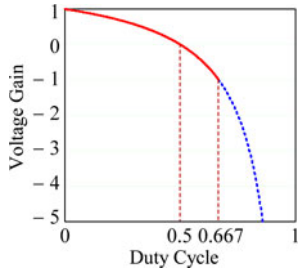

Fig. 5. Duty cycle operation region of the proposed semi-Z-source inverters (solid red line).

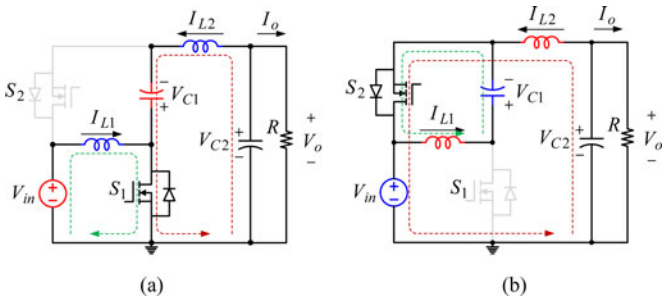

Fig. 6. Semi-quasi-Z-source operation modes in one switching period. (a) State I S_1 is ON. (b) State II S_2 is ON.

control strategy can be used to output the sinusoid voltage. Because the voltage gain of the proposed semi-Z-source inverter is not a straight line as the full-bridge inverter, a modified SPWM strategy has to be used in order to output the sinusoid voltage, which will be discussed in detail in the next two sections.

III. Operating Principle of Semi-Z-Source Inverters

Fig. 5 shows the voltage gain curve of the proposed semi-Z-source inverters. The y-axis is the voltage gain of the inverter, and the x-axis is the duty cycle of switch S_1. Switches S_1 and S_2 are conducted in a complementary manner. By operating switch S_1 with duty cycle changing from 0 to 2/3, the proposed inverters are able to output the same voltage range ($+V_{\rm in}$ to $-V_{\rm in}$) as the full-bridge inverter, as shown in Fig. 5 with red solid line. When the duty cycle of S_1 changes from (0–0.5), the inverter can output the positive output voltage; when the duty cycle of S_1 changes from (0.5–2/3), the inverter can output the negative output voltage. When the duty cycle is equal to 0.5, the semi-Z-source inverters are able to output zero voltage.

Fig. 6 shows the two states' equivalent circuit in one switching period using semi-quasi-Z-source inverter as an example for analysis. Fig. 6(a) shows state I when switch S_1 is conducted. During this period, capacitor C_1 and the input voltage source charge the two inductors, and the inductor current is increased. Fig. 6(b) shows state II when switch S_2 is conducted. During this period, the two inductors become the source and the inductor current is decreased. The inductor current reference and the capacitor voltage reference direction are marked in the figure for the following steady-state equation derivation. For more detailed dc operation modes of this circuit, the reader could refer to [87]. According to the inductor voltage second balance and the capacitor charge balance equations, we can have the following steady-state equations:

$$\frac{V_o}{V_{\rm in}} = \frac{1-2D}{1-D} \tag{1}$$

$$V_{C1} = \frac{D}{1-D} V_{\rm in} \tag{2}$$

$$I_{L2} = -I_o \tag{3}$$

$$I_{L1} = -\frac{D}{1-D} I_o. \tag{4}$$

The output voltage of the inverter can be represented by (5). And the modulation index can be defined as (6); plugging (5) and (6) into (1), we can get (7); $D' = 1-D$ is the duty cycle of S_2 as derived in (8). Because the relationship between the full-bridge inverter output and input voltage is linear in terms of switch duty cycle, the sinusoid output voltage can be achieved by using a sinusoidal changed duty cycle. But the output voltage and the input voltage of the semi-Z-source inverter are no longer in a linear relationship with the switch duty cycle. In order to achieve the sinusoid output voltage, the duty cycle cannot be changed in a sinusoid manner. A corresponding nonlinear revised duty cycle has to be used to generate the correct sinusoid output voltage. A new duty cycle reference, as shown in (7) or (8), has to be used. The comparison of the proposed modulation method for semi-Z-source inverters and the traditional single-phase Z-source inverter modulation method will be discussed in detail in the next section:

$$V_o = V \sin \omega t \tag{5}$$

$$M = \frac{V}{V_{\rm in}} \tag{6}$$

$$D = \frac{1 - M \sin \omega t}{2 - M \sin \omega t} \tag{7}$$

$$D' = \frac{1}{2 - M \sin \omega t}. \tag{8}$$

IV. Modulation of Semi-Z-Source Inverters

Fig. 7 shows the traditional single-phase Z-source H-bridge inverter and its modulation method. Simple boost control is used as an example. The correct conduction time of each switch of two-phase legs is generalized by two sinusoid voltage references compared with a triangle carrier voltage. The two sinusoid voltage references v_A^* and v_B^* are 180° phase shift from each

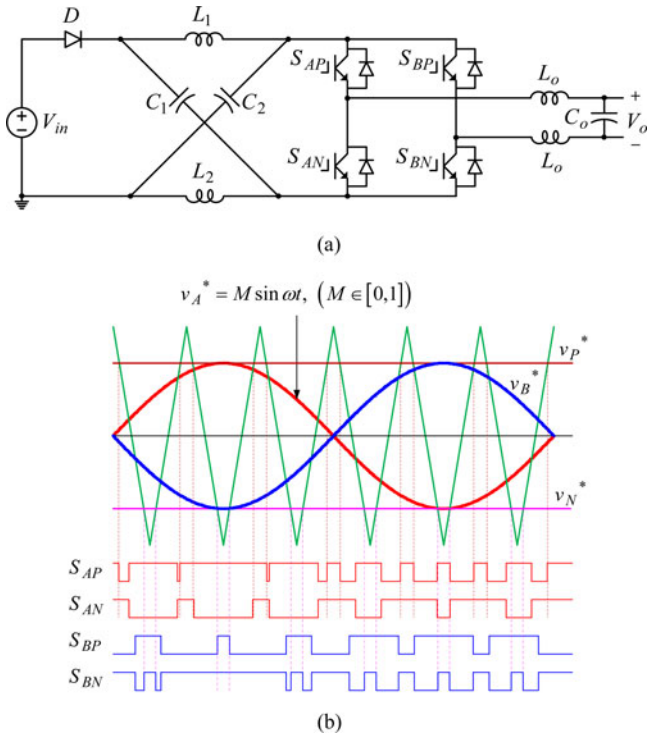

Fig. 7. Traditional single-phase Z-source H-bridge inverter and its modulation method.

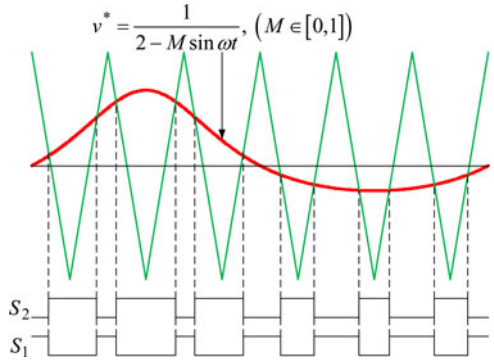

Fig. 8. Proposed modified SPWM method for semi-Z-source inverters.

other. Two straight lines v_P^* and v_N^* are used to generalize the shoot-through zero state. When the carrier is higher than the upper straight line, phase leg A goes to shoot-through state, whereas phase leg B goes to shoot-through state when the lower straight line is greater than the carrier [71]. By controlling the shoot-through duty cycle, the traditional Z-source inverter can achieve the different voltage gain. Fig. 8 shows the proposed modified SPWM method of semi-Z-source inverters. Instead of using the sinusoid voltage reference, a modified voltage reference as derived in (8) is used as the reference signal for the conduction of switch S_2 in order to output the sinusoid voltage. When the reference is greater than the carrier, switch S_2 is turned ON; otherwise, S_2 is turned OFF. And the gate signal of S_1 is complementary with switch S_2. The modified voltage reference as derived in (7) can be also used directly to generate the gate signal of S_1. But in real implantation, the gate signal

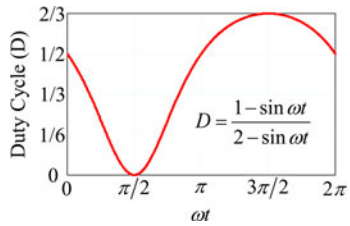

Fig. 9 Duty cycle operation region of semi-Z-source inverters when the modulation index is equal to 1.

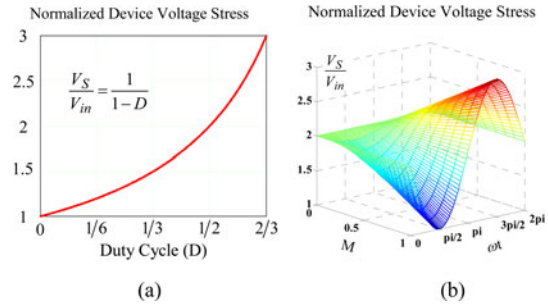

Fig. 10. Normalized device voltage stress. (a) Versus D. (b) Versus M and ωt.

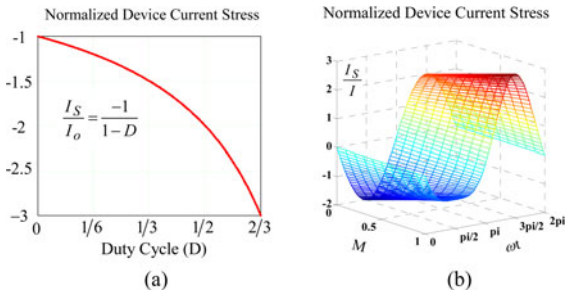

Fig. 11. Normalized device current stress. (a) Versus D. (b) Versus M and ωt.

generation of S_2 needs less calculation of DSP, which is usually preferred. So Fig. 8 uses the generation of gate signal S_2 as an example The modulation index of the modified SPWM method is also in the range of 0–1. Fig. 8 shows the situation when the modulation index $M = 2/3$ as an example. Fig. 9 shows the duty cycle operation region with different output voltages when the modulation index is equal to 1. The x-axis of Fig. 9 is the output voltage angle ωt. As shown in (5), with the change of ωt, the sinusoidal output voltage can be achieved. It can be shown from Fig. 9 that in order to output the sinusoid voltage, the duty cycle D is limited in the region (0–2/3). The other region of the duty cycle can also be utilized in other application by using at least two semi-Z-source inverters together, which will be discussed further in section VI.

V. Device Stress Analysis and Passive Component Design

The semi-quasi-Z-source inverter, as shown in Fig. 4(b), is used as an example for the device stress analysis and passive component design. The switch voltage stress can be derived as (9). Assume the output current is (10) as an example, which is in phase with the output voltage. The switch current stress can be

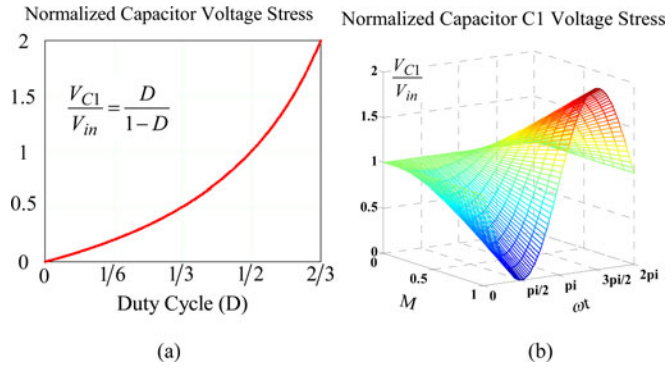

Fig. 12. Normalized capacitor C_1 voltage stress. (a) Versus D. (b) Versus M and ωt.

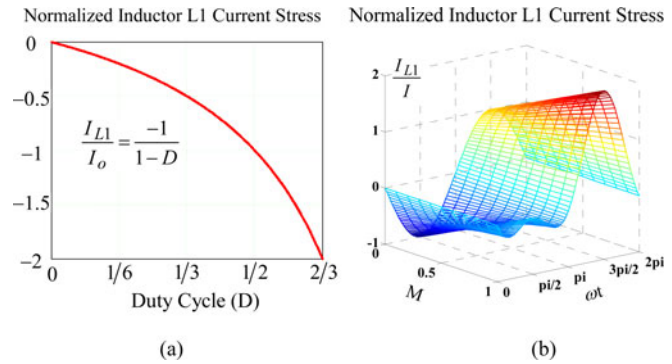

Fig. 13. Normalized inductor L_1 current stress. (a) Versus D. (b) Versus M and ωt.

derived as (11). Figs. 10 and 11 show the normalized device voltage stress and current stress versus duty cycle D, versus modulation index M and output voltage angle ωt. According to (9), (11), Figs. 10 and 11, the peak voltage across the device happens when $D = 2/3$, or $M = 1$, $\omega t = 3\pi/2$, which is $3V_{\rm in}$. And the peak current through the device also happens when $D = 2/3$, or $M = 1$, $\omega t = 3\pi/2$, which is $3I$. The voltage stress of the switching device of this inverter is high, but the switching device number is reduced; this inverter is especially suitable for low-cost micro-inverter application with high-voltage SiC switching devices [88], [89]:

$$V_S = V_{\rm in} + V_C = \frac{1}{1-D}V_{\rm in} = (2 - M\ \sin\ \omega t)V_{\rm in} \tag{9}$$

$$I_o = I\ \sin\ \omega t \tag{10}$$

$$I_S = I_{L1} + I_{L2} = \frac{-1}{1-D}I_o = -(2\ \sin\ \omega t - M(\sin\ \omega t)^2)I. \tag{11}$$

Fig. 12 shows the normalized capacitor C_1 voltage stress in terms of duty cycle, modulation index, and output voltage angle. The capacitor C_1 peak voltage is $2V_{\rm in}$ according to (2), which happens when the S_1 duty cycle $D = 2/3$. The inductor L_2 current is derived in (3), and the inductor L_1 current can be derived as (13) by plugging (7) into (4). Fig. 13 shows the normalized inductor L_1 current stress in terms of duty cycle, modulation index, and output voltage angle. The inductor L_1 peak current

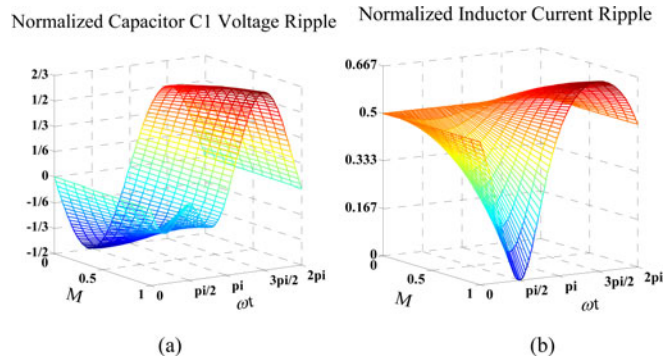

Fig. 14. Normalized capacitor C_1 voltage ripple and inductor L1 current ripple versus M and ωt.

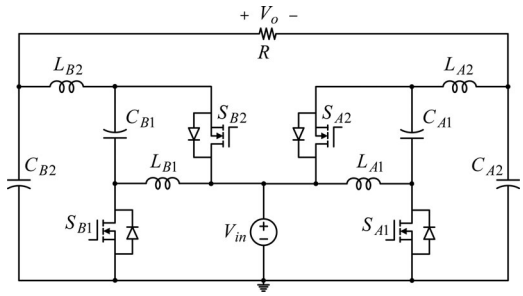

Fig. 15. Two-phase semi-quasi-Z-source inverter.

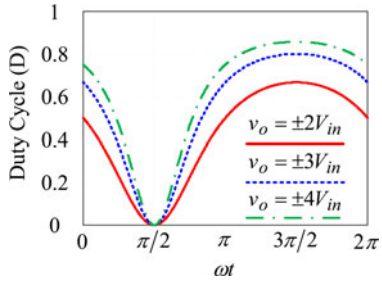

Fig. 16. Modified reference signal for two-phase semi-quasi-Z-source inverter with higher output voltage.

is $2I$, which is two times of the output current peak current. It also happens when the S_1 duty cycle $D = 2/3$. The capacitor C_1 voltage ripple can be derived as (14). And the inductor current ripple can be derived as (15) assuming $L_1 = L_2$. Fig. 14(a) shows the capacitor C_1 normalized voltage ripple versus modulation index M and output voltage angle ωt. Fig. 14(b) shows the inductor L_1 normalized current ripple versus modulation index M and output voltage angle ωt. So, the L_1 inductance value and C_1 capacitance value can be chosen according to the peak ripple requirement as shown in (14), (15), and Fig. 14:

$$V_{C1} = \frac{D}{1-D}V_{\rm in} = (1 - M\ \sin\ \omega t)V_{\rm in} \tag{12}$$

$$I_{L1} = \frac{D}{D-1}I_o = -(\sin\ \omega t - M(\sin\ \omega t)^2)I \tag{13}$$

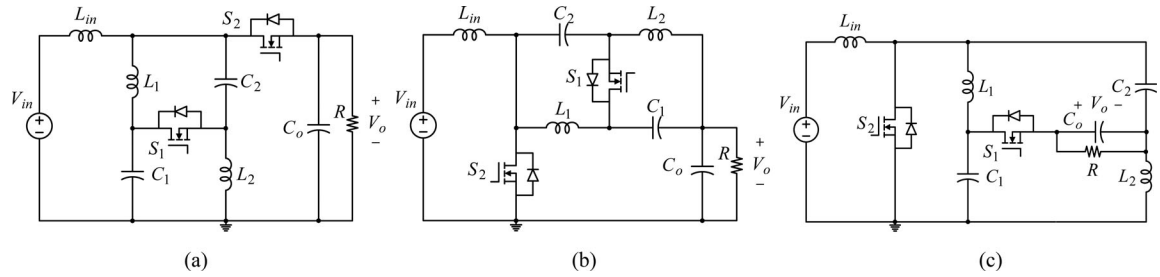

Fig. 17. Other single-phase semi-quasi-Z-source inverter topologies derived from the current-fed quasi-Z-source inverter topology.

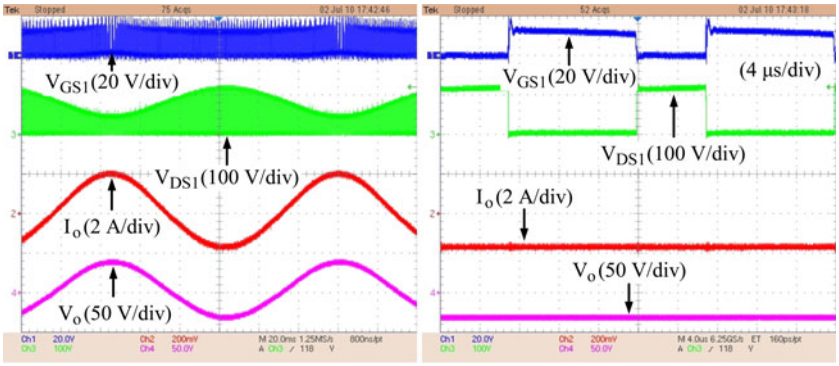

Fig. 18. Device gate to source voltage, drain to source voltage, output voltage, and output current.

$$\Delta V_{C1} = \frac{(1-D)T_s I_{L1}}{C1} = \frac{-\sin\omega t + M(\sin\omega t)^2}{2 - M\sin\omega t}\frac{T_s}{C1}I \tag{14}$$

$$\Delta I_{L1} = \Delta I_{L2} = \frac{V_{\text{in}} T_s D}{L_1} = \frac{V_{\text{in}} T_s}{L_1}\frac{1 - M\sin\omega t}{2 - M\sin\omega t}. \tag{15}$$

VI. Topology Expansion and Discussion

The proposed single-phase semi-Z-source inverter can be expanded to two-phase or three-phase inverter very easily, which are similar to boost or buck–boost inverters. The voltage gain of two-phase or three-phase semi-Z-source inverter can also be increased, because the operation range of the duty cycle can be increased from (0–0.667) to (0–1). Fig. 15 shows the two-phase semi-quasi-Z-source inverter as an example, which can also be used in the split single-phase application. The corresponding modified reference signal with different voltage gain is shown in Fig. 16. The output voltage of a two-phase semi-quasi-Z-source inverter is twice bigger than the full-bridge inverter with the same input voltage, if the voltage reference is the same with the single-phase version. By changing the voltage reference due to Fig. 16, the output voltage of a two-phase semi-quasi-Z-source inverter can be increased more. Due to the page limit, the details of circuit operation and modulation strategy of a multi-phase semi-Z-source inverter will be discussed in the future papers.

Actually, many other dc–dc converters with similar voltage gain curves of quasi-Z-source dc–dc converters, as shown in Fig. 3(b), can also be used as a single-phase inverter with modified SPWM strategy. The current-fed Z-source dc–dc converter mentioned in [78] and [85] can be used as a single-phase inverter, which has already been mentioned in the aforementioned papers. Fig. 17 shows some other single-phase inverter topologies derived from the current-fed quasi-Z-source inverter topology [57], [58]. These topologies working as a dc–dc converter have already been mentioned in [90]. There are more topologies with the similar voltage gain curves with the proposed single-phase semi-Z-source inverters that can be used as an inverter with similar modified PWM method. Due to the page limit, those topologies are not listed here.

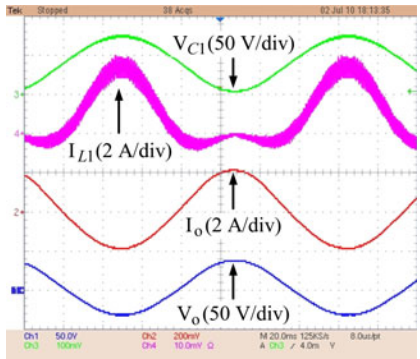

Fig. 19. Capacitor C_1 voltage, inductor L_1 current, output voltage, and output current.

VII. Experimental Results

A 40-W semi-quasi-Z-source inverter prototype with 40 V input voltage and 28 V output voltage for operation validation purposes is built. The switching frequency of the prototype

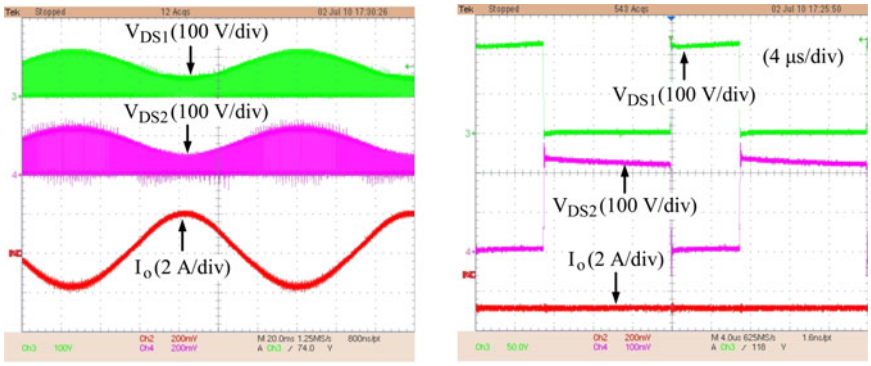

Fig. 20. Two switching devices drain to source voltage and output current.

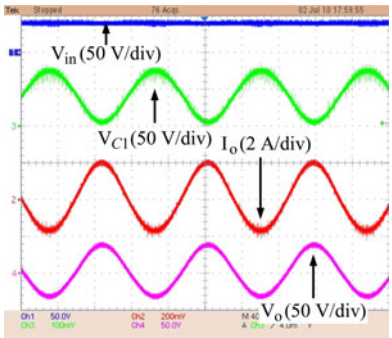

Fig. 21. Input voltage, capacitor C_1 voltage, output voltage, and output current.

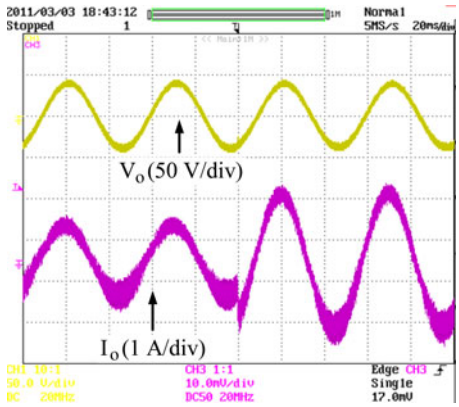

Fig. 22. Output voltage and current waveform with load step change from half power to full power.

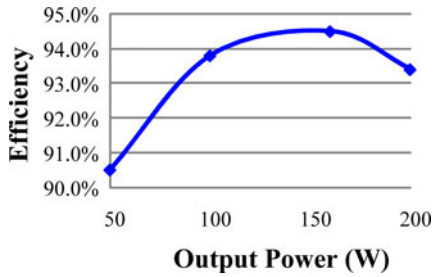

Fig. 23. Measured efficiency curve.

is 50 kHz. Because the maximum device stress is 120 V as shown in Fig. 10, two MOSFETs from ST (STP75NF20) with 200 V voltage rating are selected to be the switching device. The inductors L_1 and L_2 are designed using (13), (15), Figs. 13, and 14. Because the peak value of the load current is 2 A for the designed prototype, the peak value of the inductor L_1 current is 4 A according to Fig. 13, the inductor current ripple of L_1 is designed to be 1/3 of the peak current which is about 1.33 A. So the inductance of inductor L_1 can be calculated using (15), which is 400 μH. Inductor L_2 can be designed using the same design procedure which is also 400 μH. Capacitor C_1 can be designed using (12), (14), Figs. 12, and 14. Because the peak voltage stress of capacitor C_1 is 80 V according to (12), the multilayer ceramic capacitor (MLCC) from TDK (C5750×7R2E105K) is selected. The voltage ripple of capacitor C_1 is limited to 8.3% of the capacitor voltage; the capacitance can be calculated using (14), which is 4 μF. The output capacitor C_2 can be designed using the similar procedure which is also 4 μF.

Figs. 18–21 show the experimental results of a 40-W semi-quasi-Z-source inverter prototype. The input voltage is 40 V, the modulation index is 0.95, and the load resistance is about 19 Ω Fig. 18(a) shows the switch S_1 gate to source voltage $V_{\rm GS1}$, the switch S_1 drain to source voltage $V_{\rm DS1}$, the output voltage V_o, and the output current I_o. Fig. 18(b) shows the zoomed in waveform of Fig. 18(a). Fig. 19 shows the capacitor C_1 voltage waveform V_{C1}, the inductor L_1 current waveform I_{L1}, and the output voltage and current. Fig. 20(a) shows the two switches drain to source voltage ($V_{\rm DS1}$ and $V_{\rm DS2}$) and the output current. Fig. 20(b) shows the zoomed in waveforms of Fig. 20(a). Fig. 21 shows the input voltage $V_{\rm in}$, capacitor C_1 voltage, output current, and output voltage waveforms. Fig. 22 shows the load step change waveform when the load current is changed from half power to full power.

Compared to the traditional single-phase Z-source inverters, as shown in Fig. 7(a), the proposed semi-Z-source inverter only utilizes two switches instead of four switches and one diode. So the total cost of a semi-Z-source inverter is reduced. The Z-source network of the semi-Z-source inverter is in ac side, while the traditional single-phase Z-source inverter has the Z-source network in dc side. The total size of the Z-source network of

the semi-Z-source inverter is reduced significantly compared to the traditional single-phase Z-source inverter. Therefore, the semi-Z-source inverter is more suitable in a single-phase PV application than the traditional single-phase Z-source inverter.

A 200-W prototype with 160 V input voltage and 110 V output voltage for low-voltage grid-connected application is built. The design procedure is similar to the aforementioned 40-W prototype. The switching frequency is 20 kHz. The switching devices are STP42N65M5 from ST. The inductance of inductors L_1 and L_2 is about 1.3 mH. The capacitance of capacitors C_1 and C_2 is 1 μF. The measure efficiency curve of this prototype is provided, as shown in Fig. 23. The efficiency of this prototype is not very high due to the limitation of the laboratory supply; more efficient design can be made by optimal designed inductor and switching devices.

VIII. Conclusion

In this paper, several single-stage single-phase nonisolated semi-Z-source inverters are proposed. They are especially suitable for a PV panel in low-voltage grid-connected application as a low-cost micro inverter with high-voltage SiC switching devices. By employing the Z-source or quasi-Z-source network, the proposed inverters are able to utilize only two active switching devices to achieve the same output voltage as the traditional full-bridge inverter does. Different from the traditional single-phase Z-source inverter with an extra shoot-through zero state to achieve the boost function, the two switches of the semi-Z-source inverter are controlled complementarily. The input dc source and the output ac voltage share the same ground, which effectively eliminates the leakage current caused by the PV panel. A modified SPWM method is also proposed to solve the nonlinear voltage gain problem of the semi-Z-source inverter. The topology expansions are summarized; many other inverter topologies can be derived based on the same idea. A single-phase semi-Z-source inverter prototype has been built and tested to verify the validity of the proposed circuit and to demonstrate the special features. A 200-W prototype with 110 V output voltage for low-voltage grid-connected application has also been built; experimental results are provided.

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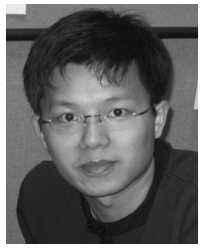

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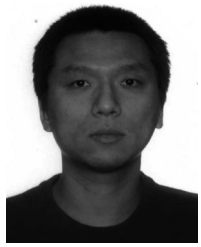

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